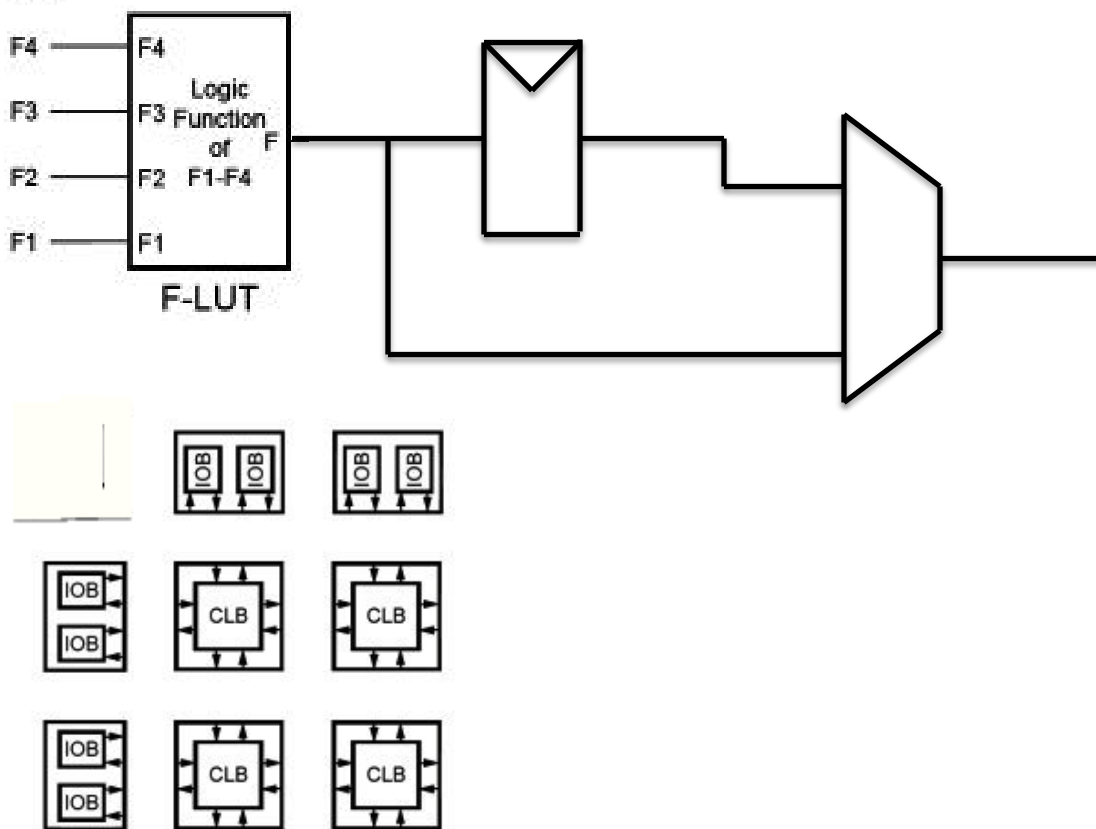


Homework 3 Due Wed May 2

Q1) Implement a one-bit half-adder using the given 2x2 array of Configurable Logic Block (CLBs). The CLB design uses just one 4-bit LUT, one flip-flop, and one mux, shown below.

You only need to specify the values that need to be programmed into the LUT and the wiring of the CLBs so that you half-adder functionality, taking in the inputs A, B and outputting the sum and carry. Write out any assumptions. (See Harris and Harris Section 5.6.2).



Q2) How is carry look ahead adder topology different from ripple carry adder? Draw the schematic for a 2 bit adder -both carry look ahead and ripple carry. (Note: Use Full adder blocks for adder circuitry and logic gates for the carry.)

b) If delay in generating carry through a one bit FA is 10 ms, what is the delay in the both the 2 bit adders? (Note: Explain your reasoning; no points will be given for answers turned in without sufficient explanation.)

Useful Source:

<http://www.cs.umd.edu/class/sum2003/cmsc311/Notes/Comb/lookahead.html>