# CSE352 Autumn 2013 Homework #2

Instructor: Mark Oskin
TAs: Vincent Lee, Mark Wyse

Due In Class 10/18/2013
Version 1.1

Please write your name and student ID at the top right corner of each page, and staple or paperclip your work together. We are NOT responsible for losing papers that were not stapled or paperclipped together.

Complete the following questions. Please write legibly and try to draw clean diagrams. Spaghetti wiring in circuit diagrams is difficult to grade. We will not grade work that is too heavily encrypted for us to read (i.e. we can't read it, we can't grade it). Please consider typesetting your work if you think that it may not be legible to the grader. You are encouraged to collaborate with your peers but you must turn in your own work. Justice will be enforced if you are caught cheating.

## Problem 1 *Warm Up*

Consider the following two implementations of a 32-bit accumulator circuit which takes a 32-bit input signal `In` and an enable signal `En` which serves as the register enable signal. Draw the timing diagrams for the signals `Acc` and `Sum` for the following set of input signals `En` and `In` signals:

| Cycle | In | En |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 1 | 1 |
| 2 | 2 | 1 |
| 3 | 3 | 0 |
| 4 | 2 | 0 |
| 5 | 4 | 1 |
| 6 | 0 | 0 |

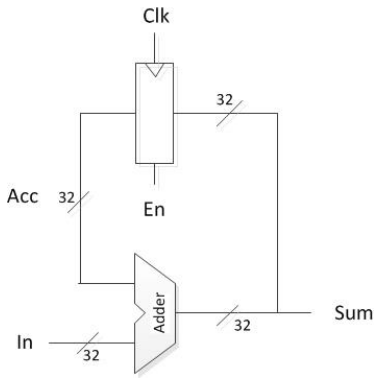



Figure 1: Accumulator A

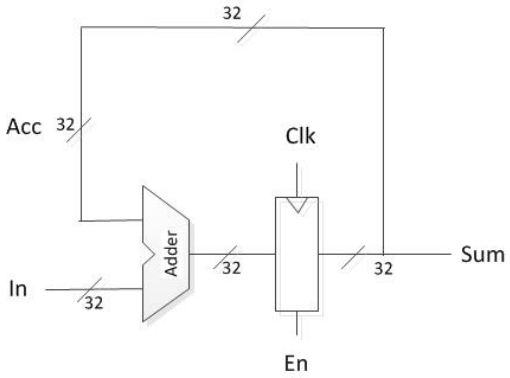
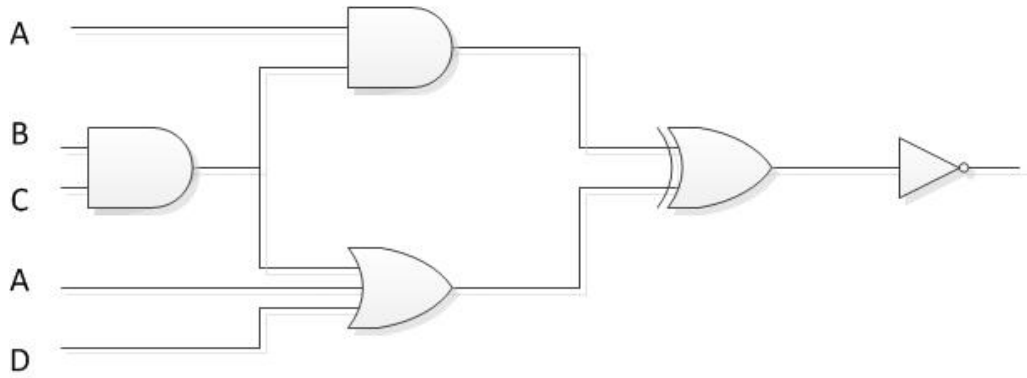



Figure 2: Accumulator B

## Problem 2 *Critical Path Delay*

Suppose we have the following circuit where the delay of an n-input gate is given by 2+2n nanoseconds.

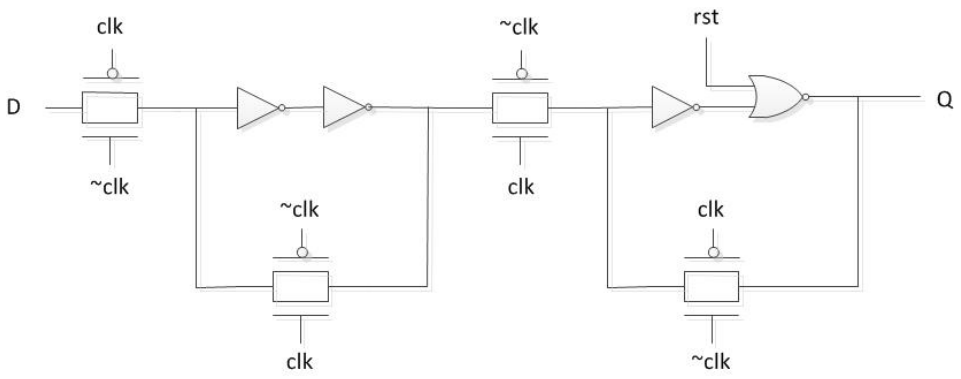



(a) What is the propagation delay of this circuit?

(b) Suppose in this system the combinational logic works out such that the input signal `A` is always 1. Can you simplify this circuit to improve the delay? If so what is the new delay?

## Problem 3 *Flip Flops*

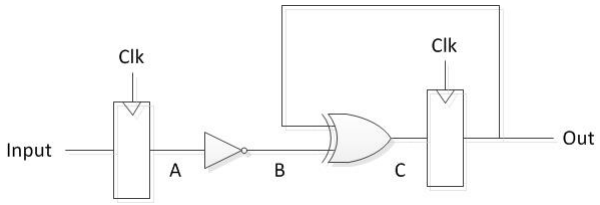
Ben Bitdiddle and Sylvia Shortcircuit are having an argument over how to implement an asynchronous reset to the following register using a signal `rst`. The asynchronous reset should immediately clear the value of the register and can be asserted for any period of time. He argues that the following modification is sufficient to implement the asynchronous reset:




Sylvia Shortcircuit disagrees and argues that Ben's solution does not actually work and that it will fail for certain cases. Who is correct? If Ben's solution is indeed incorrect, under what circumstances would his implementation fail and how would you fix it?

## Problem 4 *Timing Diagrams*

Consider the following circuit. The inverter has a combinational delay of 4ns and the XOR gate has a combination delay of 8 ns. For the registers, assume the setup time is 1.5ns, hold time is 1.5ns, and clock-to-q delay is 3 ns.




What is the maximum possible operating frequency of this circuit?

## Problem 5 *Wat Question of the Week (Optional)*

Create a Wat meme using logic gates and flip flops (https://www.destroyallsoftware.com/talks/wat).