CSE352 Spring 2014 Homework #6

Due In Class Wednesday 11/26/2014

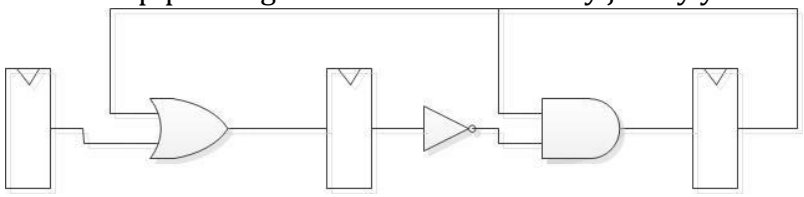
Please write your name at the top right corner of each page, and staple or paperclip your work together. We are NOT responsible for losing papers that were not stapled or paperclipped together.

Problem 1 *Pipelining Warm Up*

Using only full adders and registers design a 4-bit adder circuit that can run at 100MHz to compute the 4-bit output sum and carry out cout given two 4-bit inputs A and B. Assume the worst case propagation delay through a full adder is 7*ns*. The hold time and setup time for registers is 1*ns* and the clock-to-q delay for registers is 2*ns*. It is okay for there to be several cycles of latency before the first result appears at the output.

Problem 2 *Pipeline Placement*

Alan Turing and Edsger Dijkstra are arguing over whether the performance of the following circuit can be improved with additional pipelining. Alan argues that it is possible to improve the performance by adding another register between the AND gate and inverter. Edsger argues otherwise and claims that the structure of the circuit does not allow further pipelining. Who is correct? Briefly justify your answer.



Problem 3 *The 5 Stage Pipeline*

Ben Bitdiddle is compiling his program with NCC (Not Very Good Compiler Collection) for a 5 stage MIPS processor which **does not** use forwarding and gets the following sequence of assembly instructions:

```
addi $t0, $t0, $zero addi
$t0, $t0, 1 and $t1, $t1,
$t0 addi $t2, $t2, $zero
addi $t2, $t2, 1 sll $t2,
$t2, $t2 lui $t3, 0x1337
ori $t3, $t3, 0xCAFE
```

When he benchmarks his program he finds that his program is running poorly. How can he optimize this snippet of assembly instructions to improve the performance of his code? Write the new and improved sequence of instructions that should get him better performance.