CSE370 PAL Tutorial - Using Active-HDL to Compile to PALs

Programmable Array Logic: Specification, Compilation, and Programming

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Objectives

This tutorial will familiarize you with the process of mapping logic to a PAL and programming the PAL so that is ready to include on your protoboard along with other circuitry. In the following, a Verilog file describing a counter is used as an example. However, you'll use a Verilog file of your own to specify the logic to implemented in the PAL. After completing this tutorial you will know how to:

- Specify that a PAL is to be used to implement a block in your design;
- Instruct the tool as to the particular PAL to which the logic will be mapped;
- Run the compilation process and read the resulting reports about how the mapping proceeded including how to read the pin map for the part; and
- Program the PAL so that it is ready to be used on your protoboard.

Even though this tutorial will show you all you need to know to create basic PALs, you should experiment with Active-HDL on your own. You will find that there are many tools and options that have been left out of this tutorial for the sake of simplicity. By experimenting with these tools on your own, you will become more proficient with Active-HDL, and you may find different methods that better suit your style, while still achieving the same design goals.

Start Active-HDL

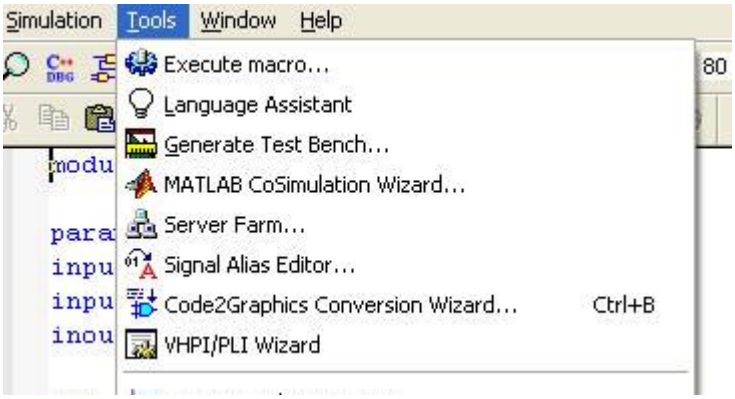
1. Open Active-HDL.
2. Select the "Open existing workspace" option and select your workspace from the previous lab in the window, or click the "More…" button to attach and open it.
3. Click OK.

* If you have forgotten how to use the "More…" button refer back to Tutorial #1 for directions.

Using a PAL in a Design

4. Go back to your Verilog design for the full-adder circuit of the Tutorial 3.

5. In the tools menu select "Preferences". There are a few steps to follow to tell ActiveHDL what type of programmable array logic you are going to use.



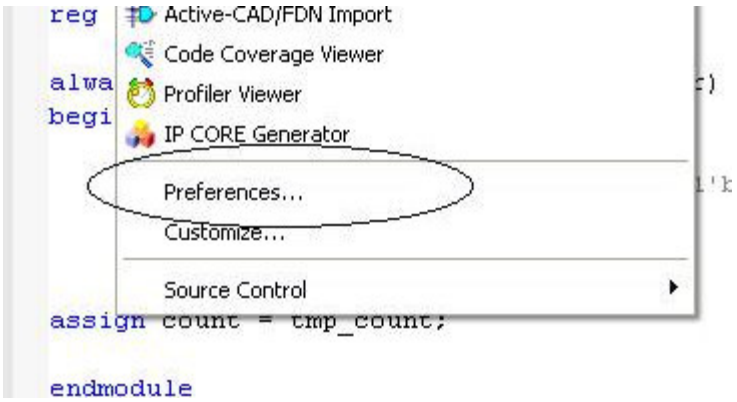


Figure 1

6. Select “Flows” from the Category list on the left. In the “Select Flow” drop down menu select “Multivendor Flow” then click OK.

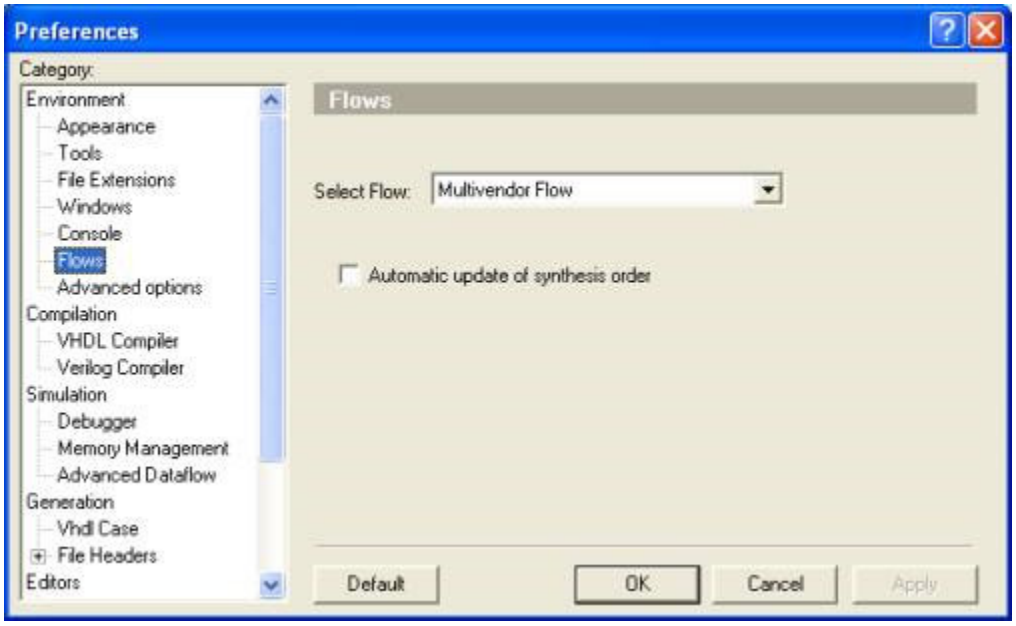


Figure 2

7. In the Design menu, select Flow Settings.

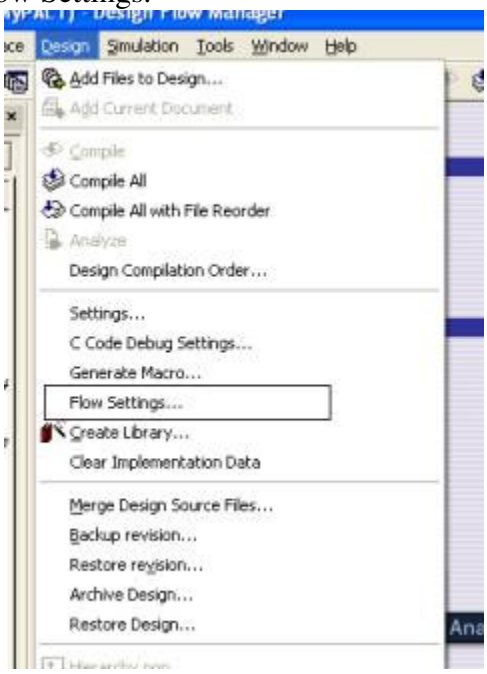


Figure 3

8. In the Flow Configuration Settings window locate the HDL Synthesis section. Change the Tool Name drop down to “Cypress Synthesis & Implementation”. In the Defaults section change the Family drop down to “Cypress SPLD.” Click OK.

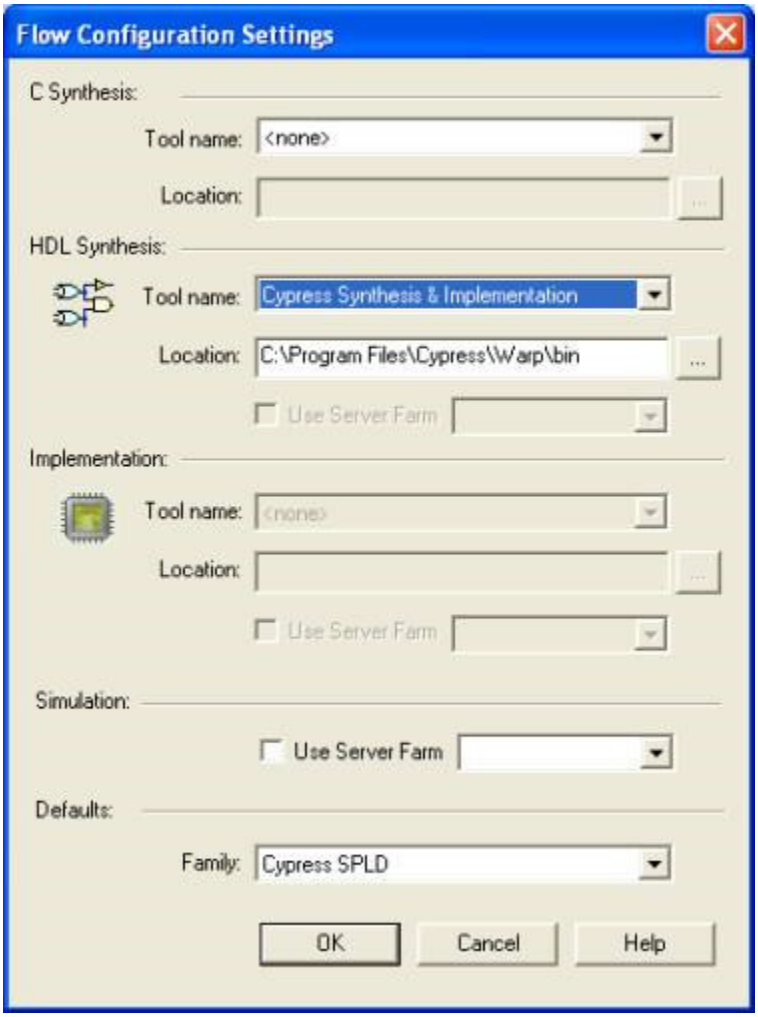


Figure 4

9. Open the design flow by clicking on the Design Flow icon in the tool bar.

Figure 5

10. In the Design Flow page to the left of the “Synthesis & Implementation” icon you will see an options button. Click the options button (Highlighted orange in Figure below).

Figure 6

11. Ensure that the Top Level Unit drop down has your Verilog file in it. If not, change it to match the file you want programmed in the PAL. Note: For a file to be listed in the Top Level Unit drop down box it must already be compiled. Change the Device drop down box to “c22v10” and the Package drop down to “PALCE22V10L-25PC”. Click OK when finished.

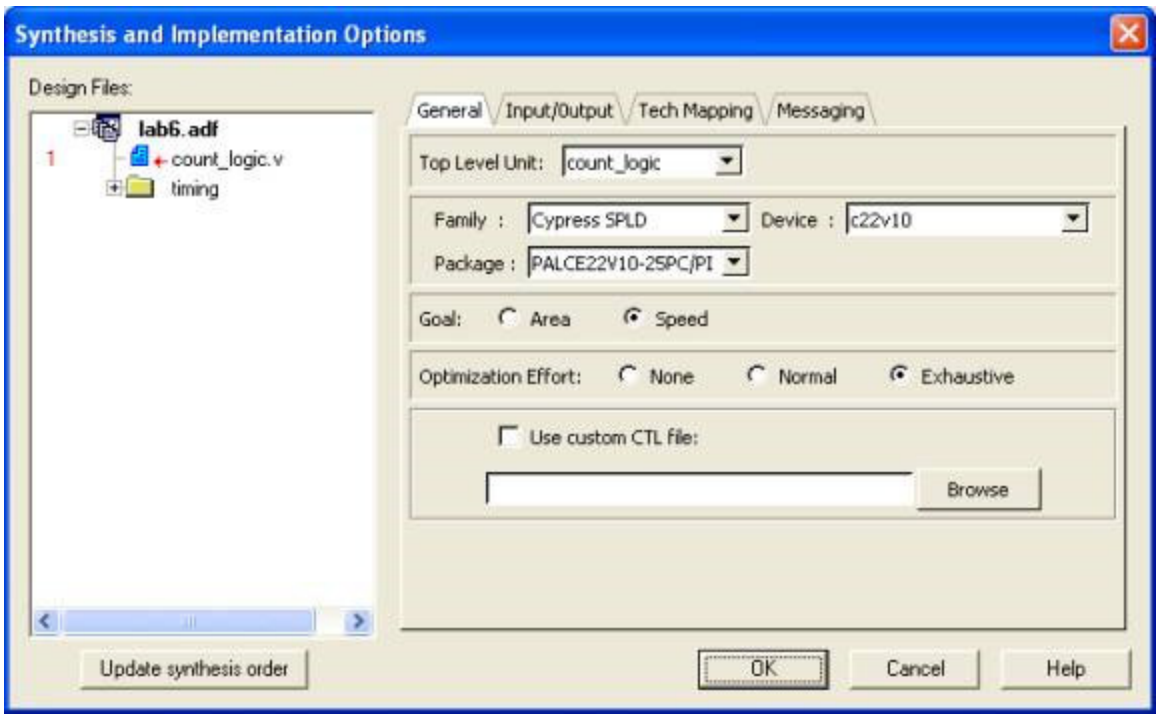


Figure 7

12. When you are ready to generate the files to program your PAL click on the “Synthesis & Implementation” icon (shown in figure below) on the Design Flow page. This will cause a file of type *.jed to be generated that can be used to program your PAL. **NOTE: Only click on the synthesis & implementation button once. You will need the log file for the next step to determine the pin configuration. If aldec starts a second synthesis it will clear the log files.** When performing a new synthesis, aldec clears the log files in preparation for the new synthesis but then does NOT perform a new synthesis because the old synthesis is up-to-date. This leaves you with a blank log file. If this happens and your log file is blank, change something in your Verilog file, save it, recompile it, then synthesis it. This will cause aldec to perform a new synthesis and generate a new log since the source file changed causing the files to be out-of-date.

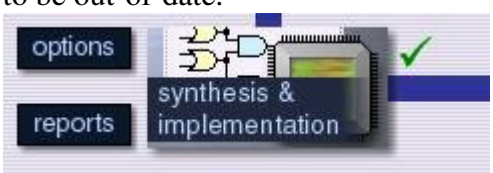


Figure 8

13. After the synthesis completes click the reports button that is located to the left of the Synthesis & Implementation button. (Highlighted orange in Figure below).

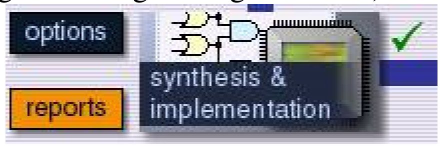
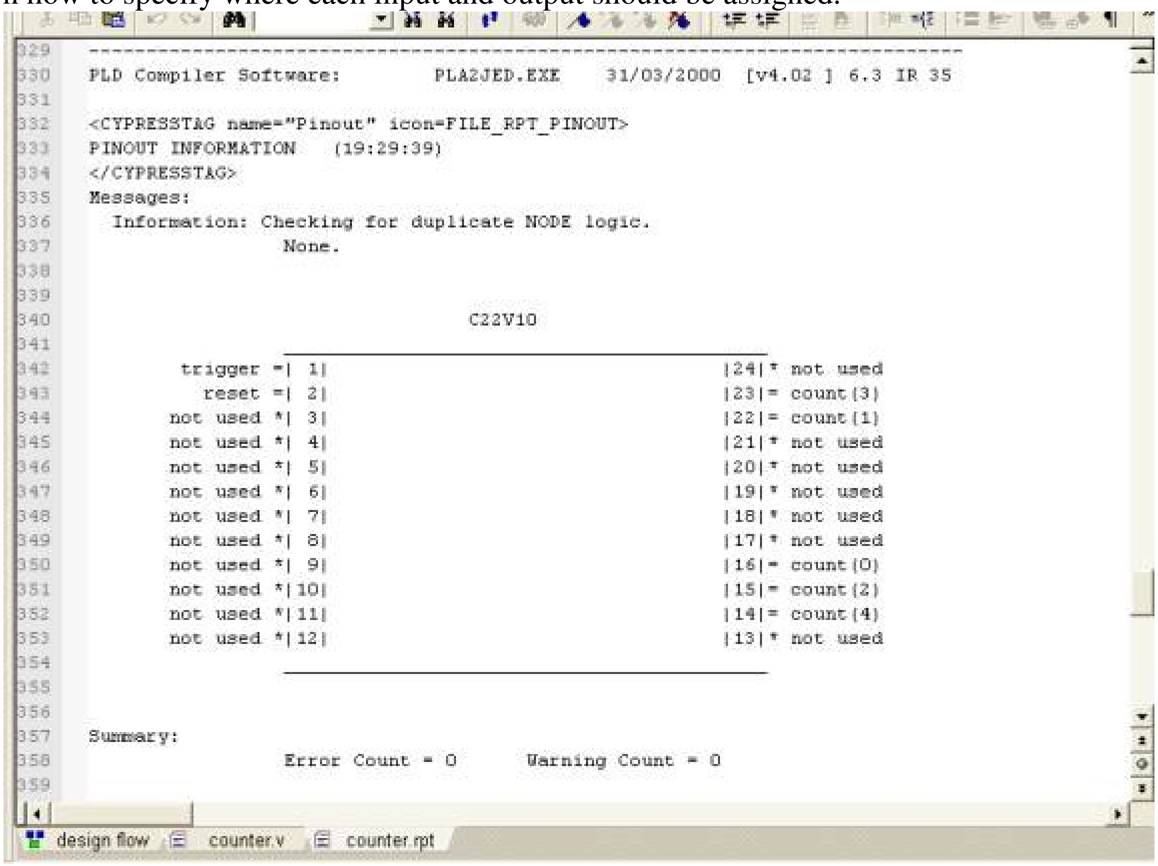


Figure 9

14. You should look at this report carefully and make sure you understand all its parts. Double click on the report for your Verilog module and scroll down until you find the diagram the displays the location of the pins. The diagram should like the figure below. **<u>NOTE: Pin 12 is GND and Pin 24 is Vcc even though they say not used.</u>** You might want to save this part of the log for future reference when you use your PAL on your protoboard. Note that the pins are assigned by the tool. In a later tutorial, we'll learn how to specify where each input and output should be assigned.



```
------------------------------------------------------------------------------
PLD Compiler Software:       PLA2JED.EXE    31/03/2000  [v4.02 ] 6.3 IR 35

<CYPRESSTAG name="Pinout" icon=FILE_RPT_PINOUT>
PINOUT INFORMATION   (19:29:39)
</CYPRESSTAG>
Messages:
  Information: Checking for duplicate NODE logic.
               None.


                                C22V10
                 __________________________________________
        trigger =| 1|                                  |24|* not used
          reset =| 2|                                  |23|= count(3)
       not used *| 3|                                  |22|= count(1)
       not used *| 4|                                  |21|* not used
       not used *| 5|                                  |20|* not used
       not used *| 6|                                  |19|* not used
       not used *| 7|                                  |18|* not used
       not used *| 8|                                  |17|* not used
       not used *| 9|                                  |16|= count(0)
       not used *|10|                                  |15|= count(2)
       not used *|11|                                  |14|= count(4)
       not used *|12|                                  |13|* not used
                 __________________________________________


Summary:
               Error Count = 0      Warning Count = 0
```


Figure 10

15. Goto the special PAL programming station in the lab and logon as the appropriate user that contains your .jed file on its network share.
16. Place your 22V10 PAL chip in the programmer. First lift the release lever so that it is pointing straight up. The TOP of the chip (end with notch) should be away from the lever(see diagram on right of programmer). Place the chip in the programmer so that the chip is as close to the lever as possible. This means that all the extra space for pins should be left towards the top of the programmer. DO NOT force the chip in. Make sure to properly align the pins. The bottom of the chip should be near the bottom of the programmer which is next to the lever. Your chip should fit in the red box shown in the diagram below. After placing the chip in the programmer close the lever.

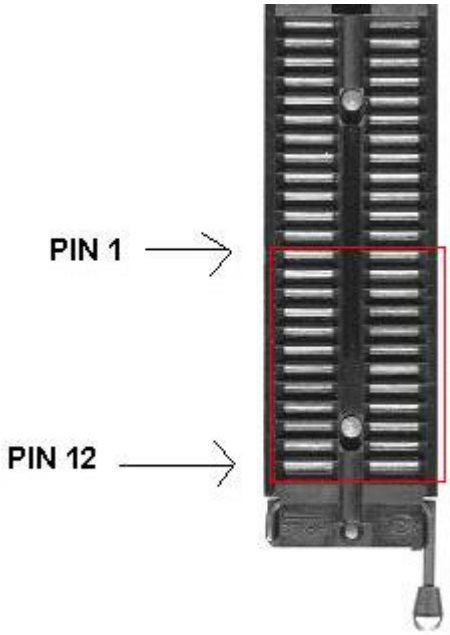


Figure 11

17. From the programs menu go to BK PRECISION and open the program BK4uw. After BK PRECISION opens and finds the programmer, verify the programmer is working by looking on the "programmer" box in the bottom of the window under status(red circle in Figure 12) it should say "ready," if it doesn't contact the course staff. **IMPORTANT:** Verify the programmer is setup for your PAL by looking at the "Device" window located at the bottom of the screen(red arrow in Figure 12) and making sure the program lists "Cypress PALCE22V10" as the Device. If the Cypress PALCE22V10 is listed SKIP step #4 and go to step #7. If another device is listed go to step #4.

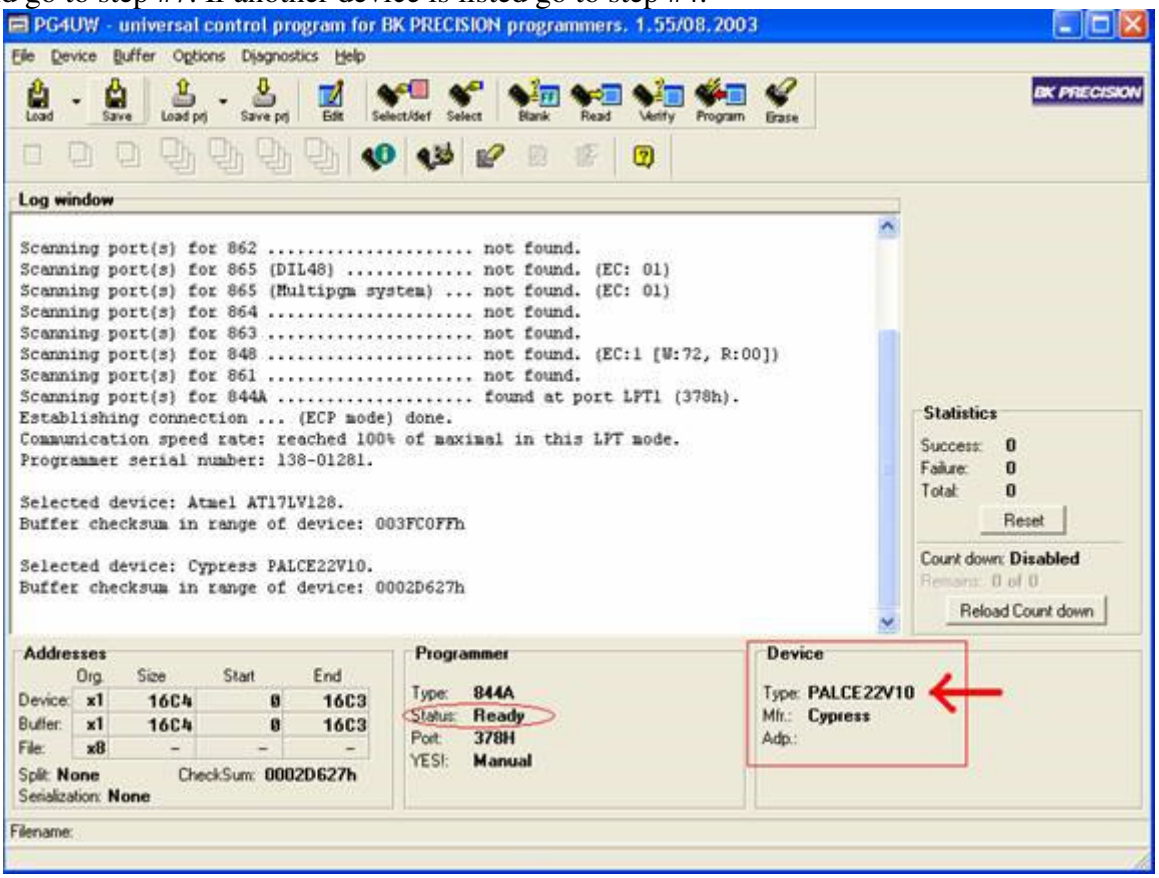


Figure 12

18. To setup the programmer to select your PAL go to the “Device” menu and click on “Select Device.” In the Select Device window (shown in figure below) type “Cypress PALCE22V10” in the Search field. There are several Cypress PALs, make sure you select “Cypress PALCE22V10.” Click OK when finished. The PAL should now show up in the Device window at the bottom of the screen should now look similar to the figure above.

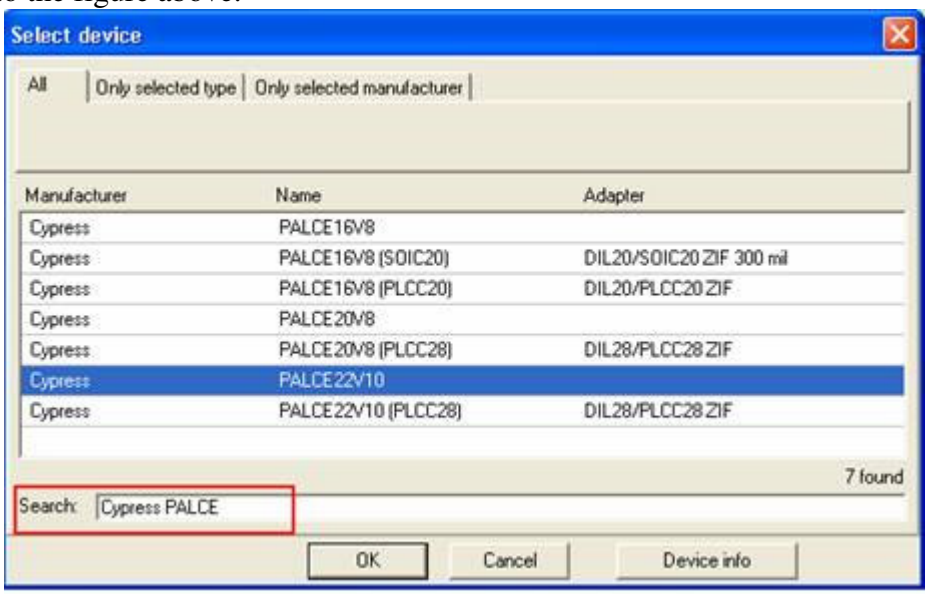


Figure 13

19. Next you will need to setup the options you will be able to perform on this chip. Select the menu option “Operation options,” which is located under the “Device” menu and the “Device options” sub menu.

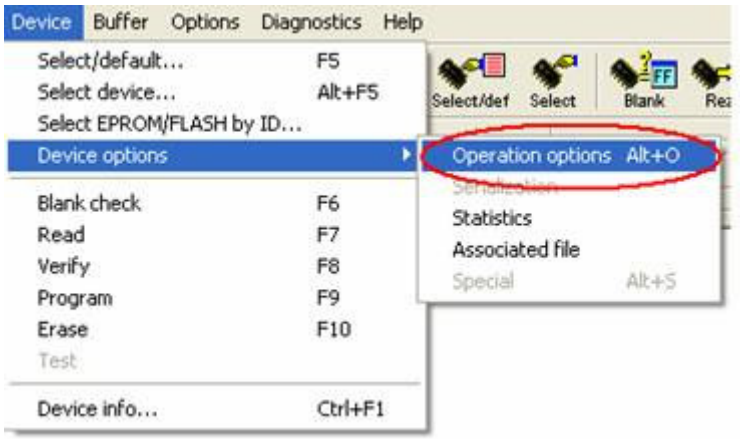


Figure 14

20. In the Device Operation Options window make sure the “Device” checkbox has a check in it. Click OK.

Figure 15

21. Select Load from the File menu and navigate to your .jed file and click open.

Figure 16

22. Click the Erase Button on the toolbar to erase the PAL 

23. Click the Program button on the toolbar to load your .jed file onto the PAL.

24. A window will appear asking for confirmation. Make sure the Device box has a check mar. If the check mark is present click YES. If a check mark does not appear, click no and go to step 5.

25. After the device finishes programming a window will come up and ask if you want to repeat this action. Click on the no button

26. Congratulations you have programmed your PAL. Remember to Exit BK PRECISION, remove the PAL from the programmer, and log out of the computer for the next person.

Concluding Remarks

You should now understand how to program a PAL to implement logic you specified in a Verilog file. You should have a sense for the tool flow that compiles a specification, a set of Boolean equations, fits them to a particular device (in this case, the 22V10), and then creates a programming file to match. You should have also learned to use the PAL programmer in the lab and have a PAL ready to use in yoiur protoboard.

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