CSE 370 Midterm 1

Winter 2009

Problem 1:

(4 pts) (a) What integer (in base 10) does the binary string 1011 represent:

(i) as an unsigned integer?

11

(ii) as a 4-bit twos complement integer?

-5

(2 pts) (b) What is $7A_{16} + 57_{16}$ in hex representation ?

$D1_{16}$

(7 pts) (c) Use De Morgan's theorem to find the complement of

$F = (A\,B + \overline{B}\,C) + B\,(\overline{C} + \overline{A})$

using negations only in literals - no double negations. Do not try to simplify further.

$\overline{F} = (\overline{A} + \overline{B})\,(B + \overline{C})\,(\overline{B} + (C\,A))$

(7 pts) (d) Simplify F = (A B + B′ C) + B (C′ + A′) as much as you can using Boolean algebra (There is no need to label the rules you use.)

F = (A B + B′ C) + B (C′ + A′)
= A B + B′ C + B C′ + B A′
= A B + A′ B + B C′ + B′ C
= (A + A′) B + B C′ + B′ C
= B + B C′ + B′ C
= B + B′ C
= B + C

Problem 2:

Consider F (A, B, C, D) = A B C + B′ C D + B D′

(7 pts) (a) Write down the Boolean expression of F in the **canonical** 'sum-of-products' (i.e. minterm) form.

F (A, B, C, D) = A′ B′ C D + A′ B C′ D′ + A′ B C D′ + A B′ C D + A B C′ D′
+ A B C D′ + A B C D
= Σ m (3, 4, 6, 11, 12, 14, 15)

(6 pts) (b) For a **canonical** 'product of sums' logic circuit, how many OR and AND gates do you need? Also specify the number of inputs for those OR and AND gates you use (so you answer should in the form of "three 3-input OR gates and two 2-input AND gates", for example. (HINT: if you are unsure, draw a schematic of the circuit so that partial credit may be given.)

Seven 4-input AND gates and one 7-input OR gate

(7 pts) (c) Now do the same as (b) for a canonical 'sum of products' logic circuit. How many OR and AND gates do you need? Also specify the number of inputs for those OR and AND gates

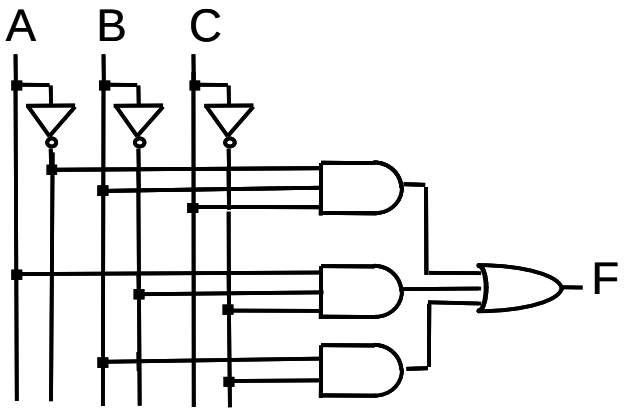
F = Π M(0, 1, 2, 5, 7, 8, 9, 10, 13)

Nine 4-input OR gates and one 9-input AND gate.

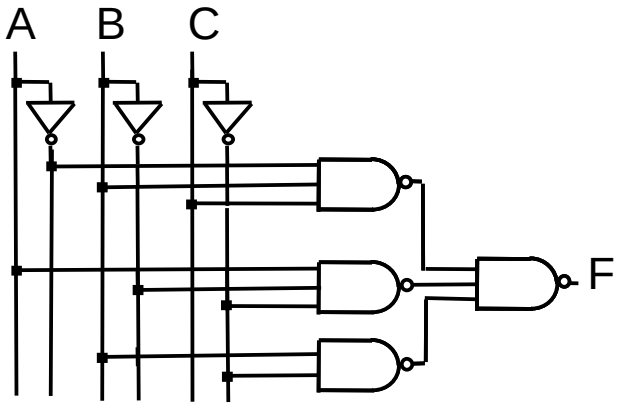
Problem 3:

Given F = A′ B C + A B′ C′ + B C′ draw a logic gate circuit for F in 'product-of-sums' form as follows:

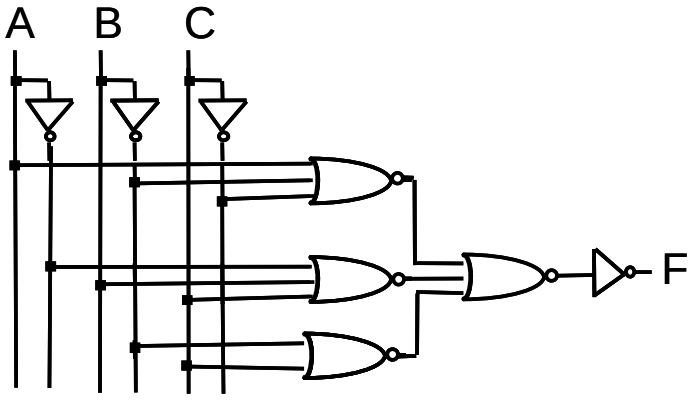
(6 pts) (a) With OR/AND gates only (can use inverters)



(7 pts) (b) With NAND gates only (can use inverters)



(7 pts) (c) With NOR gates only (can use inverters)

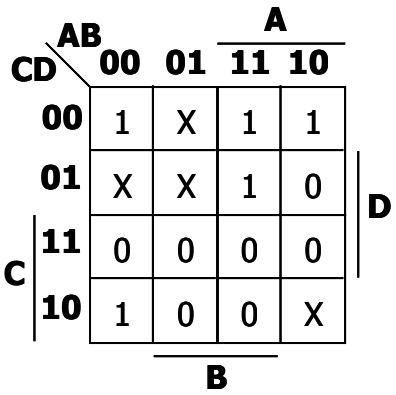


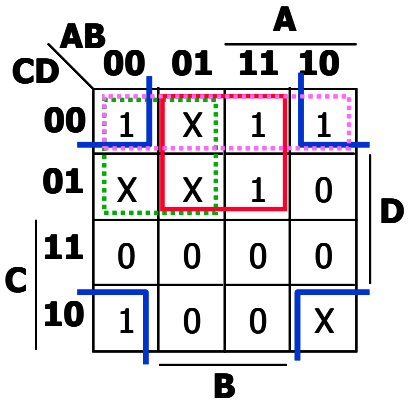
Problem 4:

For the following truth table,

(7 pts) (a) Draw the Karnaugh map for F
(7 pts) (b) Identify all the sub-cubes (max size, min number) on another copy of your K-map.
(6 pts) (c) Use this to produce a minimum 'sum of products' expression for F.

A	B	C	D	F
0	0	0	0	1
0	0	0	1	X
0	0	1	0	1
0	0	1	1	0
0	1	0	0	X
0	1	0	1	X
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	X
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0



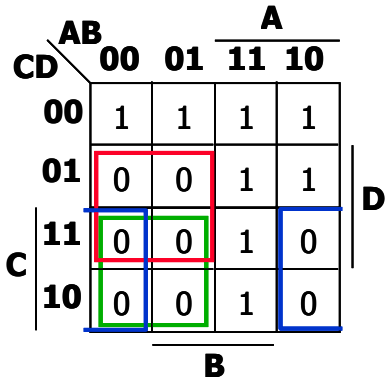


$$F = B\,C' + B'\,D'$$

Problem 5:

Solve the following questions for function F (A,B,C,D) = Π M(1,2,3,5,6,7,10,11)

(10 pts) (a) Use a K-map to write F in a minimized 'product-of-sums' form.



$$F = (A + C')\,(A + D')\,(B + C')$$

(10 pts) (a) Express F using one 8:1 Multiplexer (can use inverter gates also)