CSE370: Introduction to Digital Design
Winter 1999

Homework Set 9

DUE: Friday Mar 12, 1999, 12:30 pm

Please show *all* of your work. Solutions do not have to be typeset, but may be if desired. In any case, your solutions must be legible.

1) Katz Problem 9.5 (state reduction of fig. Ex9.5, p.489). Draw a new diagram of the reduced machine. Be sure (via naming or a brief description) that it is obvious which states you combine.

2) You are part of a team building a CPU. The CPU is to have an accumulator (AC) register that is always one of the ALU inputs, and three general-purpose registers R1, R2, and R3, which can be selected as the other ALU input. Your team has been told to use one Motorola 74-181 as the ALU, and at least one 74-170 for the registers. Links to data sheets for these chips are on the homework page. Other people on the team are designing the memory interface and the instruction fetch mechanism. Your job is:

   a) Draw a schematic showing how the ALU, register chip, and the control unit are connected. The control unit must not have any connections to the 4-bit data inputs or data outputs of the ALU or registers. Do not show or even worry about connections to PC, IR, MAR, etc. etc.

   b) Design the finite control (sequence of control signals) needed to implement a "vector add" operation. This operation sets the contents of the AC equal to the sum of the contents of R1, R2, and R3. Your control unit should not worry about decoding the instructor, updating the PC, etc – simply issue the correct signals in the correct order. Express your design in two ways as follows. In both cases, indicate the control unit outputs for every step.

      i) as a state transition diagram, giving the states descriptive or symbolic names.
      ii) as a program in an informal register transfer notation.

3) Describe at least two reasons why you might want to use static memory (SRAM) over dynamic memory (DRAM) and then give at least two reasons to choose DRAM over SRAM.