378 Final - Where: EE1 125 - When: Dec 18th 2:30 - 4:20 - Be there or Be Square

Homeworks: HW: Lecture Coverage: Purpose
        HW1: 1-2: Binary numbers
        HW2: 3-7: SPIM programming
        HW3: 2-9: Binary Translation
        HW4: 2-13: Single-cycle processor design
        HW5: 2-22: Pipelined processor design
        HW6: 2-26: Caches (and software-hardware continuum)

Lectures (Roughly)
        1 - Introduction
        2 - Architecture overview
        3 - Binary numbers
        4 - MIPS Overview
        5 - Computational instructions
        6 - Load/Store instructions
        7 - Control instructions
        8 - Misc. instructions
        9 - Procedures
        10 - Other ISA's, RISC vs. CISC
        11 - Performance Metrics
        12 - Implementation: Data path
        13 - Implementation: Control
        14 - Implementation
        15 - Microprogramming
        16 - Microprogramming
        17 - Microprogramming
        18 - Pipelining as Microprogramming
        19 - Pipelining as Microprogramming
        20 - Pipelining
        21 - Pipelining
        22 - Pipelining / VLIW / Advanced Topics
        22 - Memory Hierarchy / Caches
        23 - Caches
        24 - Virtual memory (TLBs)
        25 - Review
        26 - Review / Multiprocessors / Virtual memory / Caches
        27 - Floating point
        28 - Advanced Topic: Tomasulos Algorithm
        29 - Advanced Topic: Tomasulos Algorithm
        30 - Advanced Topic: Quantum Computing

General comments:

I don't expect you to memorize much -- this won't be a "what's on page 156?" test.

You can expect to have to demonstrate skills you learned to complete the homework. This includes skills required to debug and test your homework's.

You can expect questions that have more than one right answer.

You can expect at least one question that will cause you to think for a very long time. Do this question last.

The test will be cumulative across the entire quarter.

My advice for studying for this final is to understand all of the projects and to do the cache/TLB questions that Tim & Dmitriy handed out. This class is about doing -- particularly working on projects. So you can expect the test to also focus around this.

You should be proficient at implementation questions and understand how to modify existing code / processor wiring to create new functionality.

Be sure to practice good test taking skills. Skim the entire test first prior to starting on any questions.