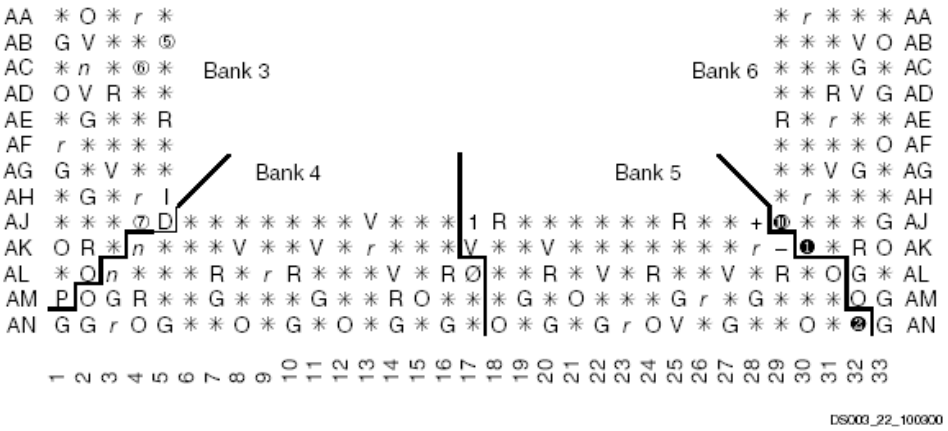
Xilinx AFX Board pinouts—1/21/03-- HWLAB



Rows AJ, AK, AL, AM, and AN are accessible

Figure 7: **BG560 Pin Function Diagram**

Pinout Diagrams

The following diagrams, CS144 Pin Function Diagram, page 17 through FG680 Pin Function Diagram, page 27, illustrate the locations of special-purpose pins on Virtex FPGAs. Table 5 lists the symbols used in these diagrams. The diagrams also show I/O-bank boundaries.

Table 5: **Pinout Diagram Symbols**

Symbol	Pin Function
✳	General I/O
❄	Device-dependent general I/O, n/c on smaller devices
V	V_{CCINT}
v	Device-dependent V_{CCINT}, n/c on smaller devices
O	V_{CCO}
R	V_{REF}
r	Device-dependent V_{REF}, remains I/O on smaller devices
G	Ground
Ø, 1, 2, 3	Global Clocks

Table 5: **Pinout Diagram Symbols** ***(Continued)***

Symbol	Pin Function
⓫, ❶, ❷	M0, M1, M2
⓾, ①, ②, ③, ④, ⑤, ⑥, ⑦	D0/DIN, D1, D2, D3, D4, D5, D6, D7
B	DOUT/BUSY
D	DONE
P	$\overline{\text{PROGRAM}}$
I	$\overline{\text{INIT}}$
K	CCLK
W	$\overline{\text{WRITE}}$
S	$\overline{\text{CS}}$
T	Boundary-scan Test Access Port
+	Temperature diode, anode
–	Temperature diode, cathode
n	No connect

Rows AJ, AK, AL, AM, and AN are accessible via the black plug-strips in front of the FPGA.