

467 Final Exam Study Guide

Exam content:

- I. A section of True/False questions covering factoids from the lectures.
- II. A section of Multiple-choice questions covering factoids from the lectures.
- III. Possible problems in the following formats:
 - a. Given a circuit schematic and timing values, complete the timing diagram to a specified resolution.
 - b. Implement the given function in the simple FPGA shown (similar to last homework).
 - c. Translate the following Verilog code into the equivalent circuit diagram.
 - d. Translate the following circuit diagram into equivalent Verilog code.
 - e. Story problem: implement solution in schematic and Verilog.
 - f. Problem dealing with waveguide model and Verilog.

Important topics:

All the (non-review) lectures, including Charlie's, are fair game.

Microblaze, Waveguides, Digital Filters, Pipelining, C-slowng, Retiming,

Clock Skew/Metastability, FPGA design for reliability

Final Exam time: **Thursday, 3/17: 8:30-10:20 a.m. ME 242**