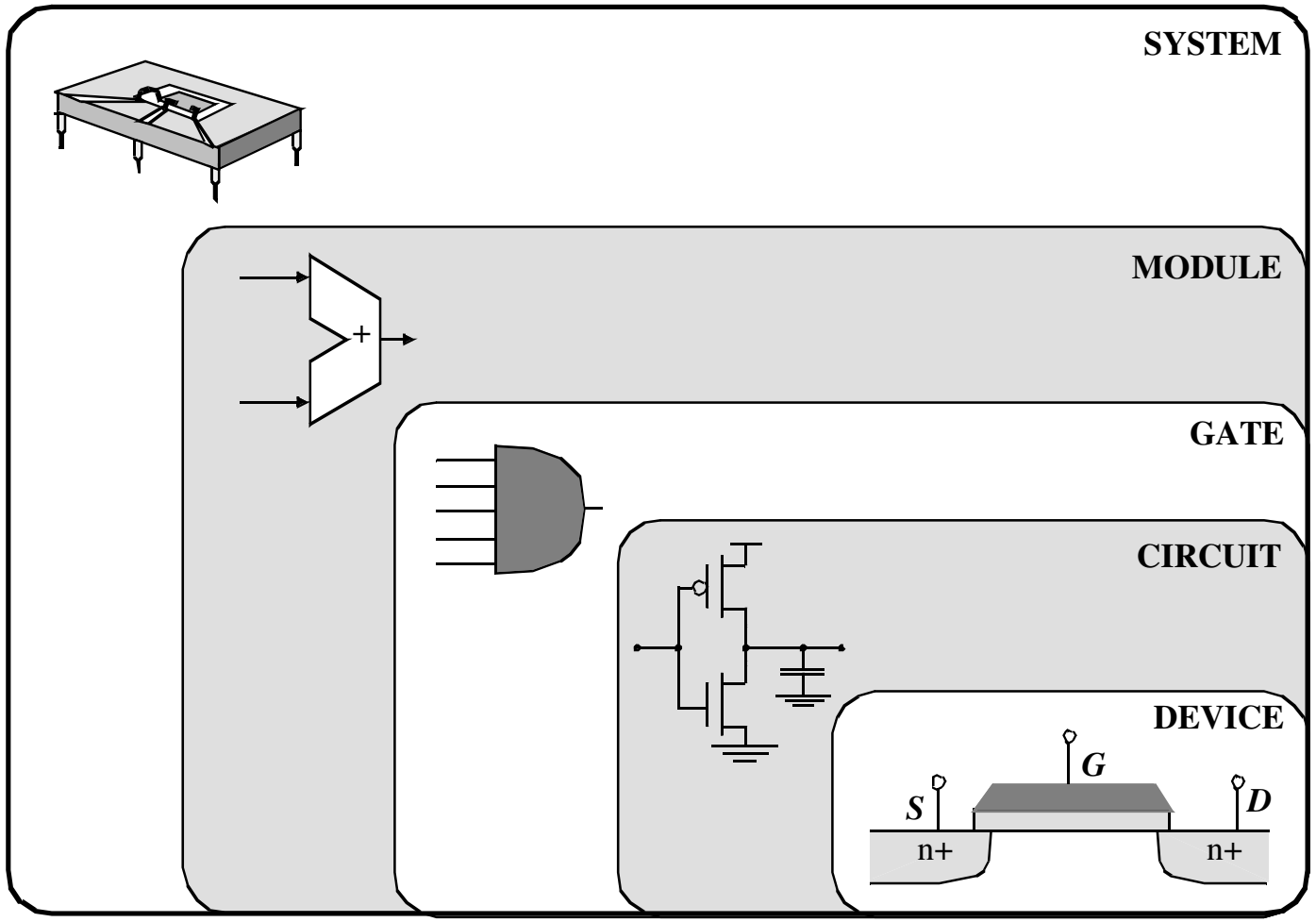
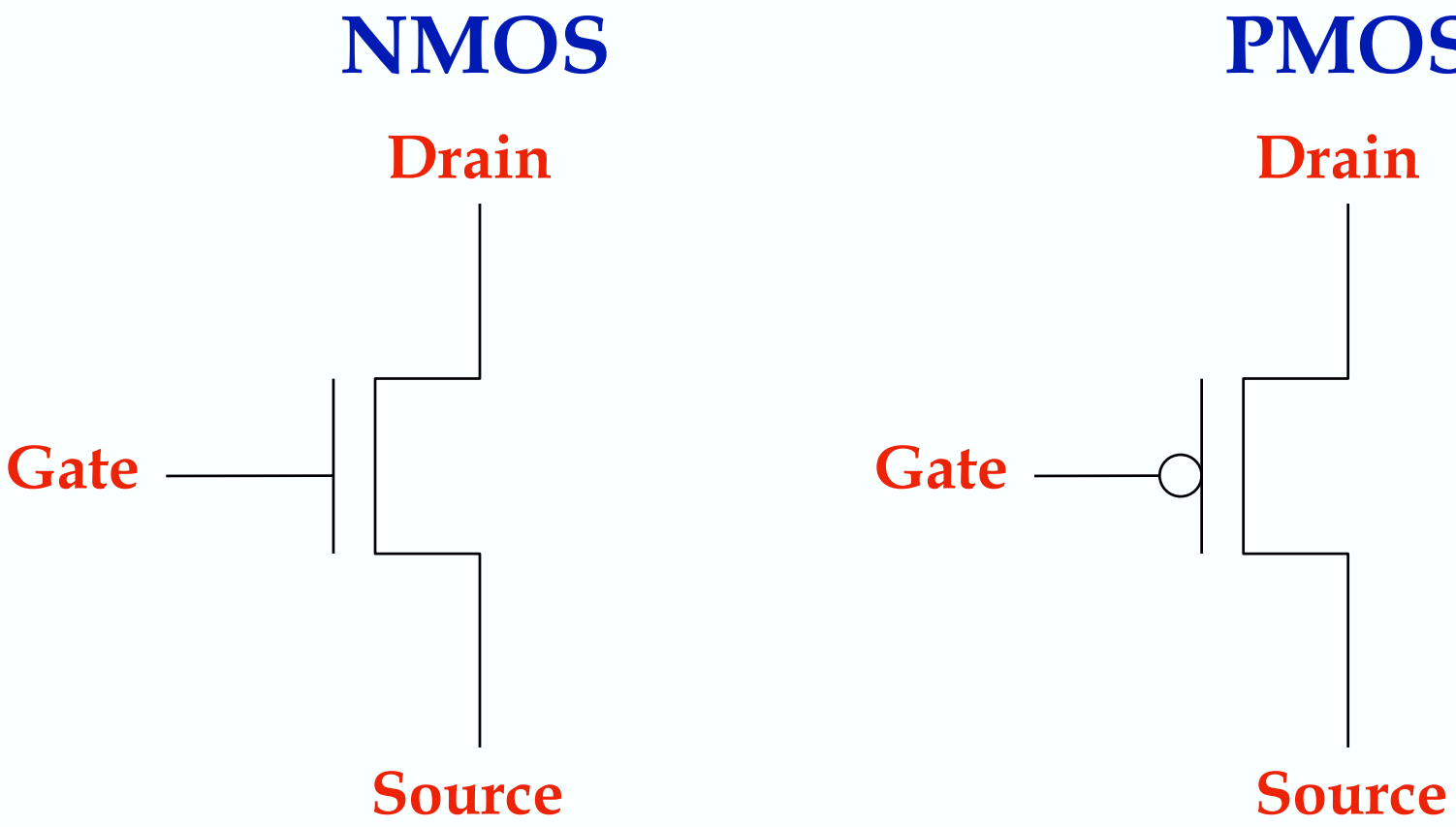
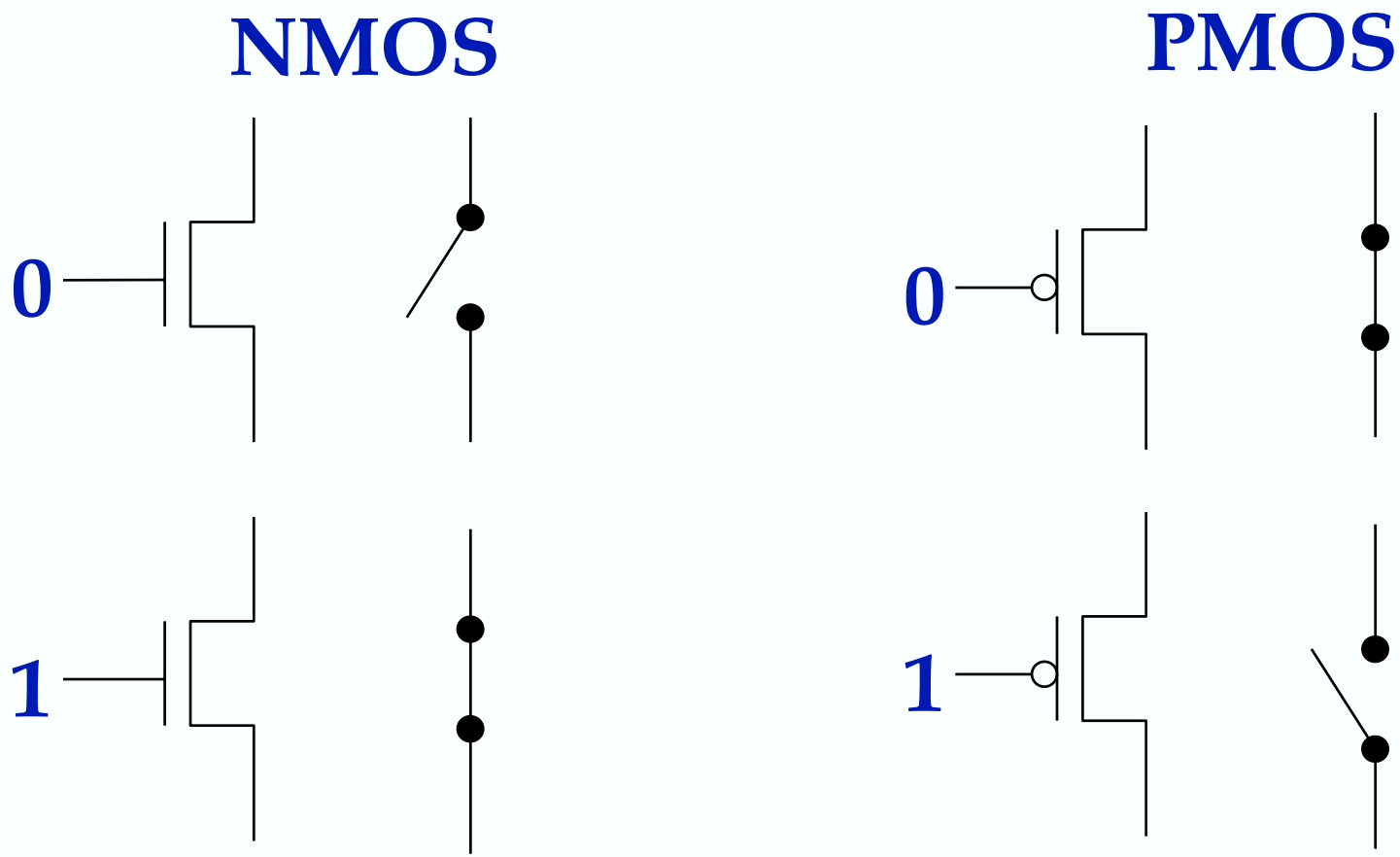
Design Abstraction Levels



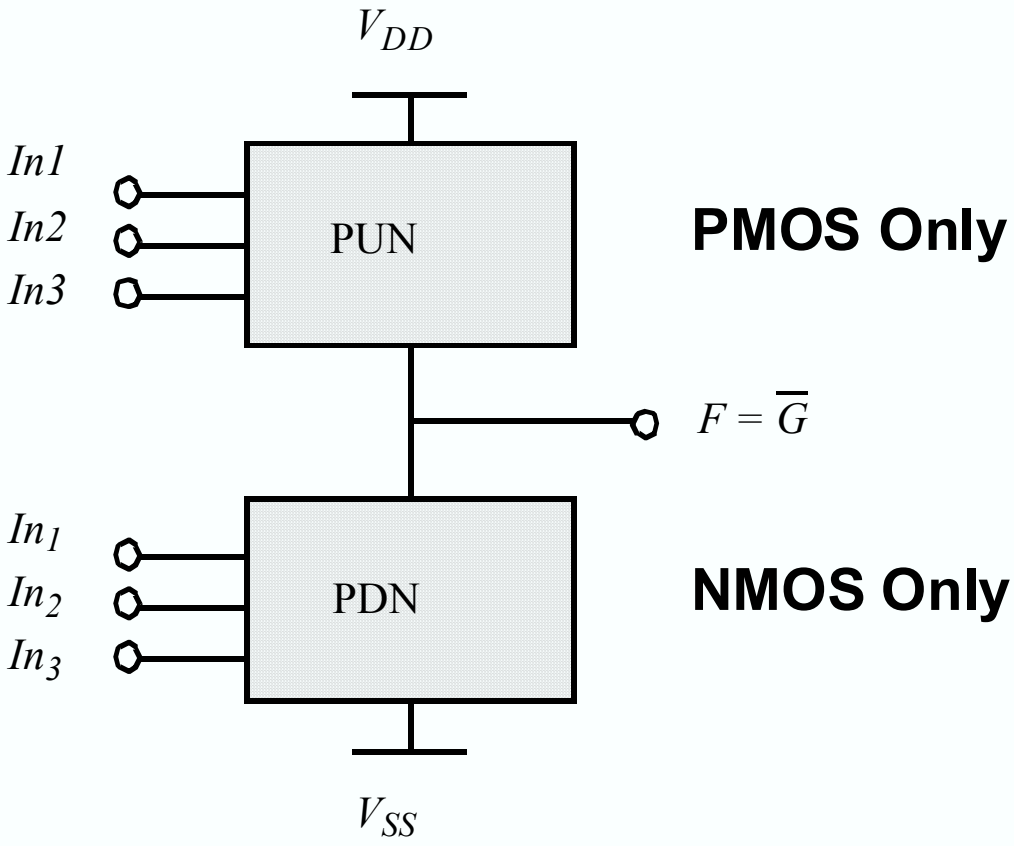
Complementary Metal-Oxide-Semiconductor (CMOS) Transistors



MOS Transistors as Switches

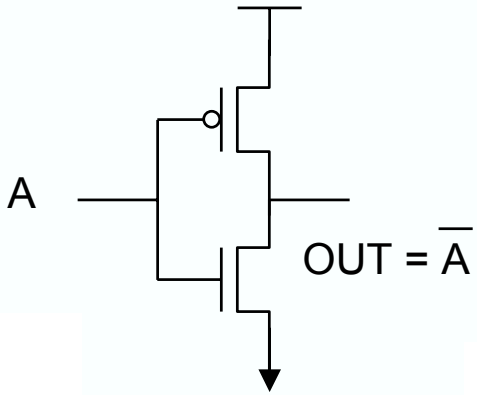


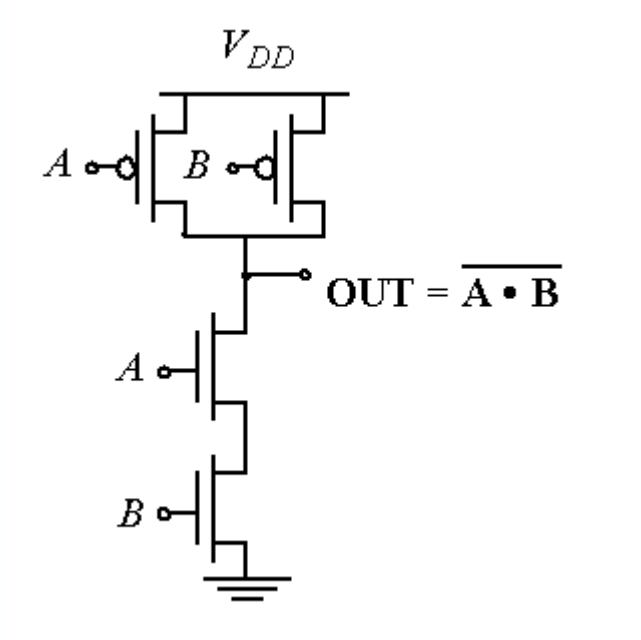
Static CMOS

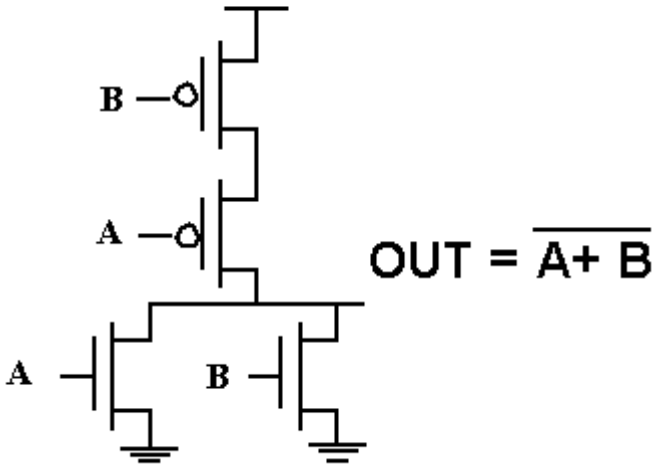


PUN and PDN are Dual Networks

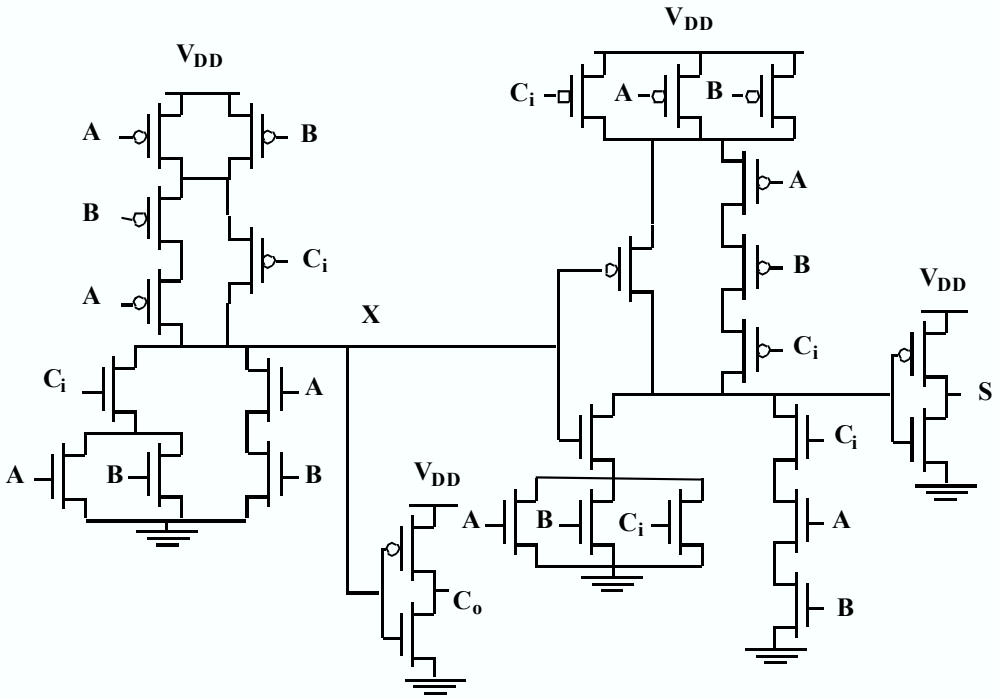
Basic Logic Gates







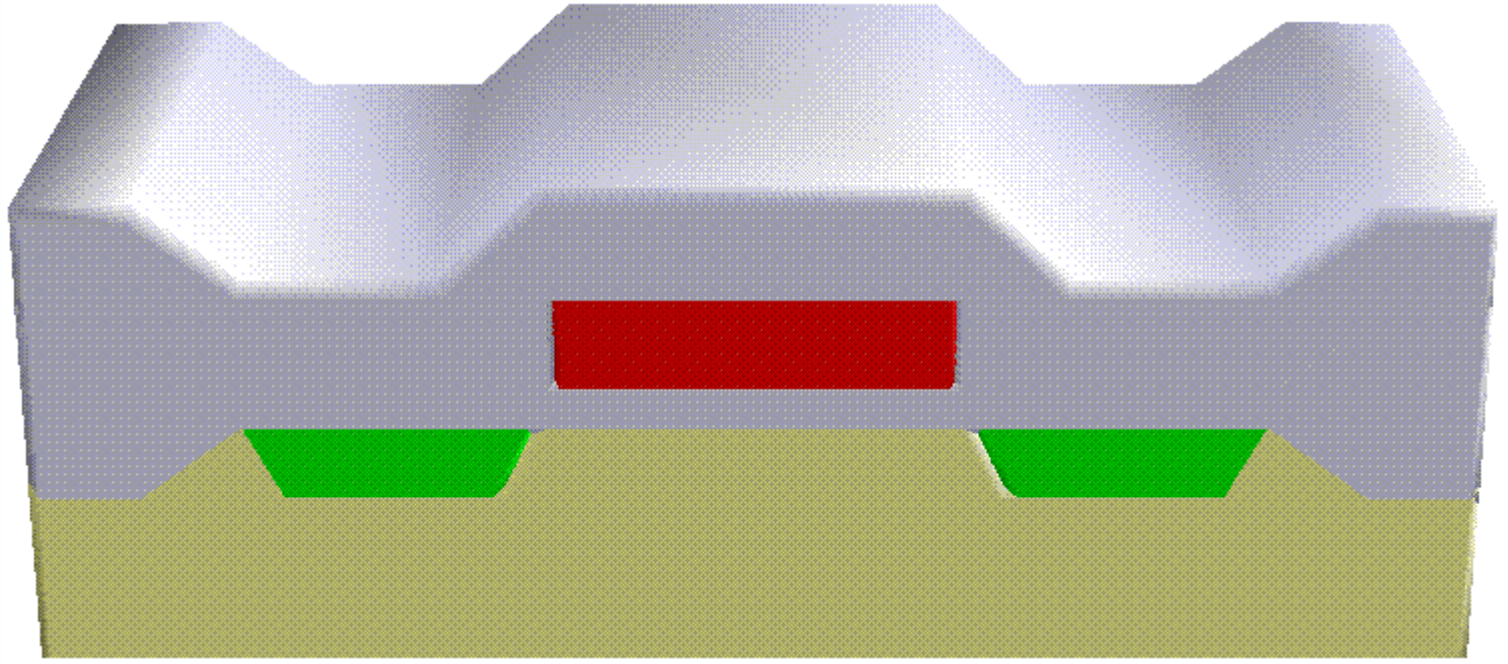
Example: Full Adder



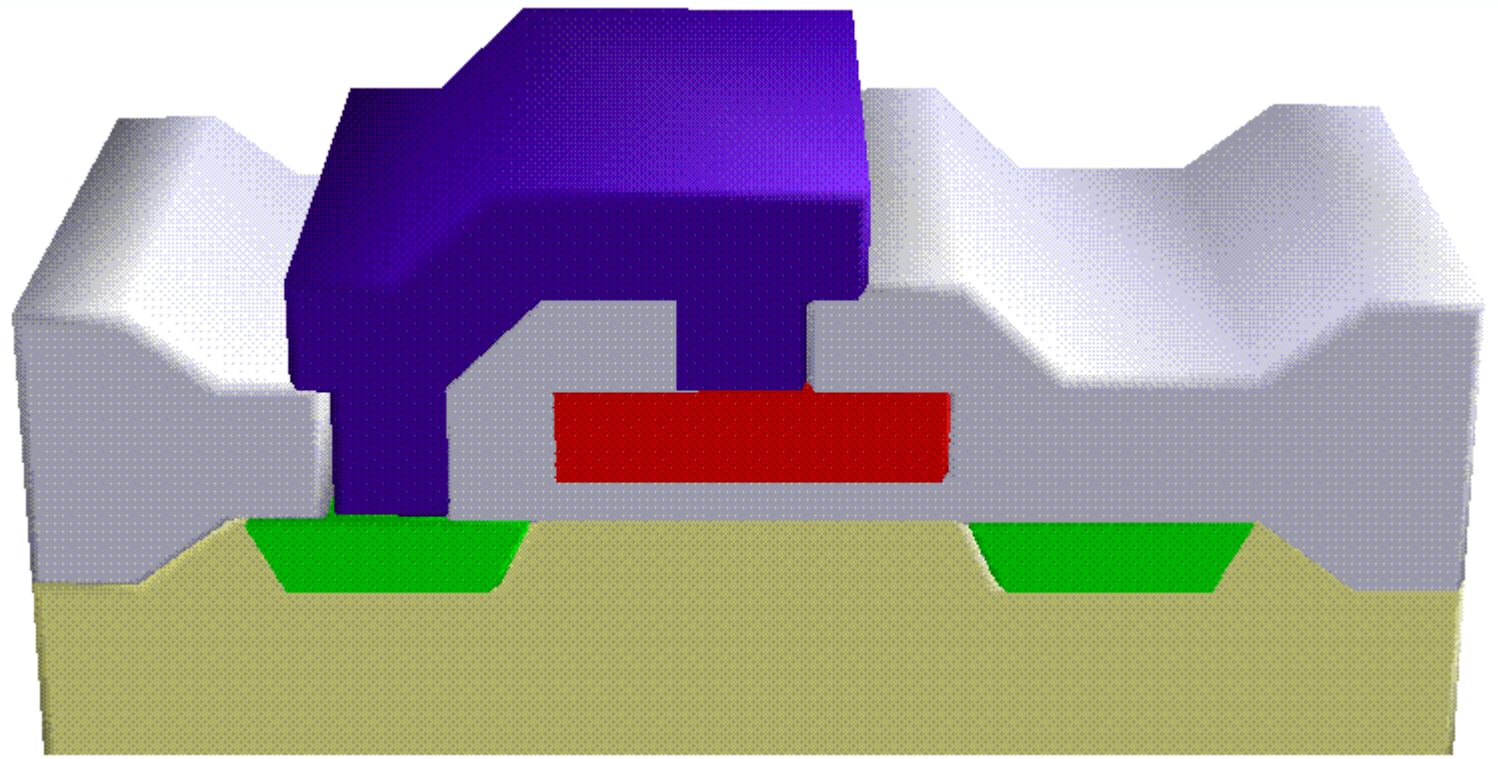
$C_o = AB + C_i(A+B)$

28 transistors

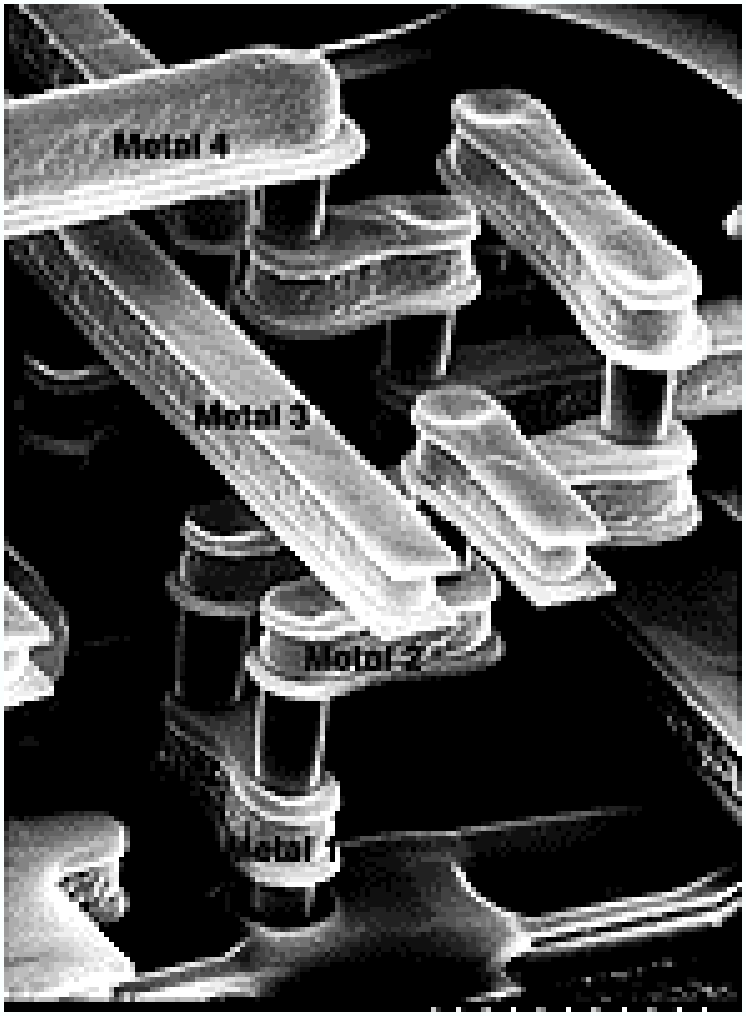
MOSFET



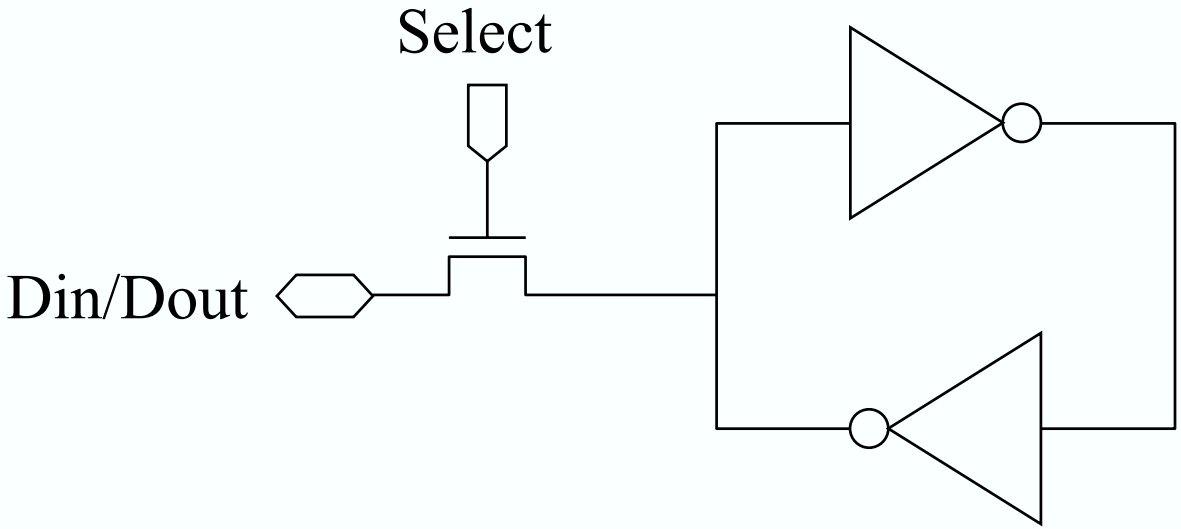
Metal Interconnect



Modern Interconnect

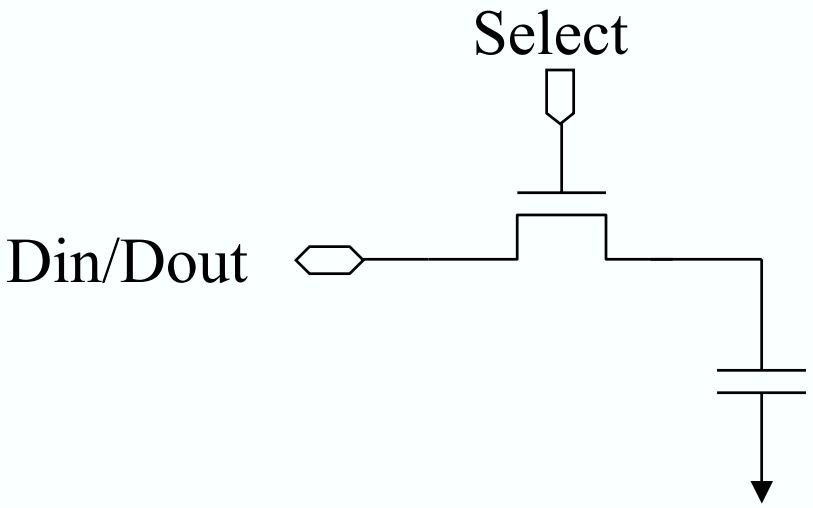


Feedback-Based Latch



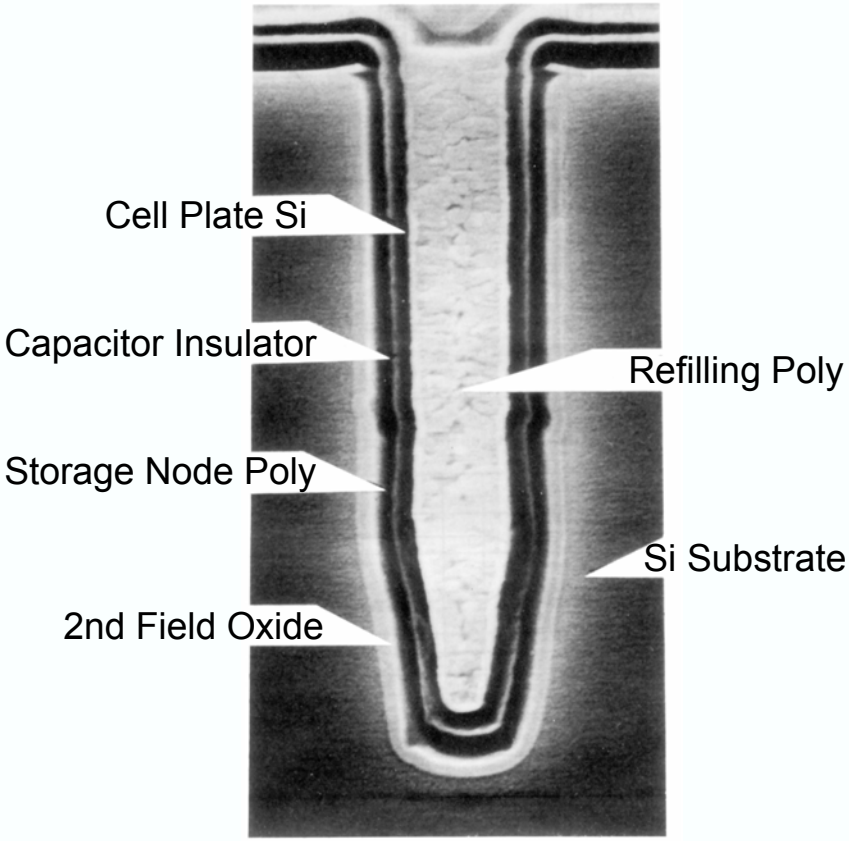
- Pro
  - » Holds data as long as power applied
  - » Actively drives output: can be made fast
- Con
  - » Big (5 transistors in this configuration)

Charge-Based Latch

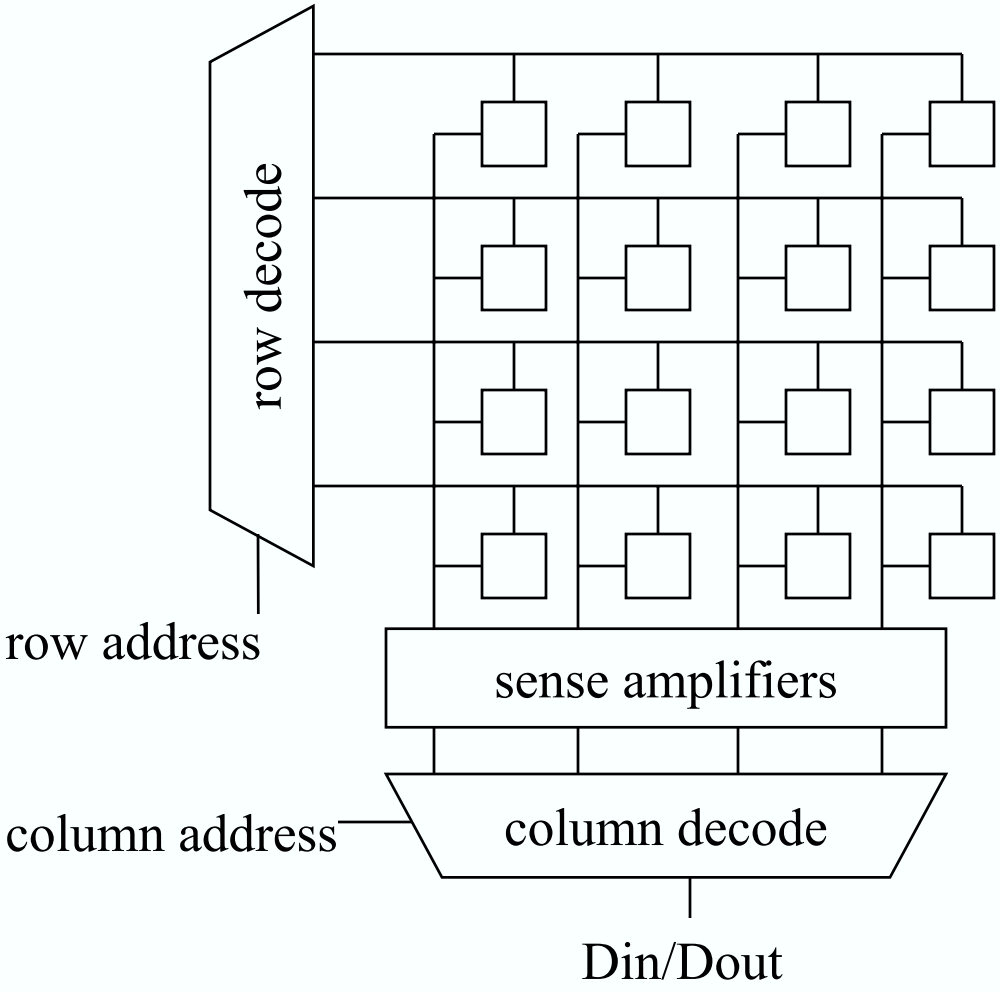


- Pro
  - » Small: 1 transistor, 1 capacitor (may be gate of transistor)
- Con
  - » Charge leaks off capacitor (~ 1 ms)
  - » Reads can be destructive and slow for large fan-out

DRAM Trench Capacitor

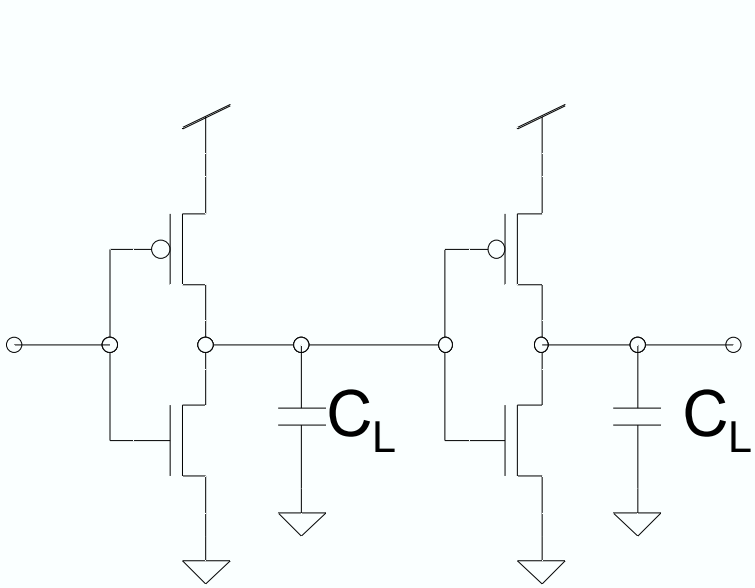


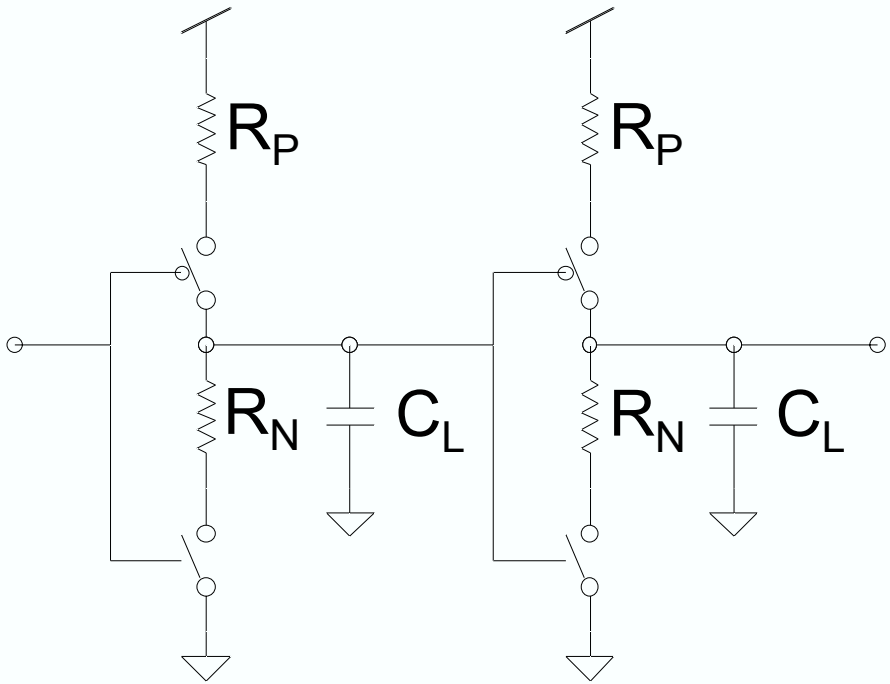
Array-Structured Memory Architecture



- All cells on selected row sensed simultaneously

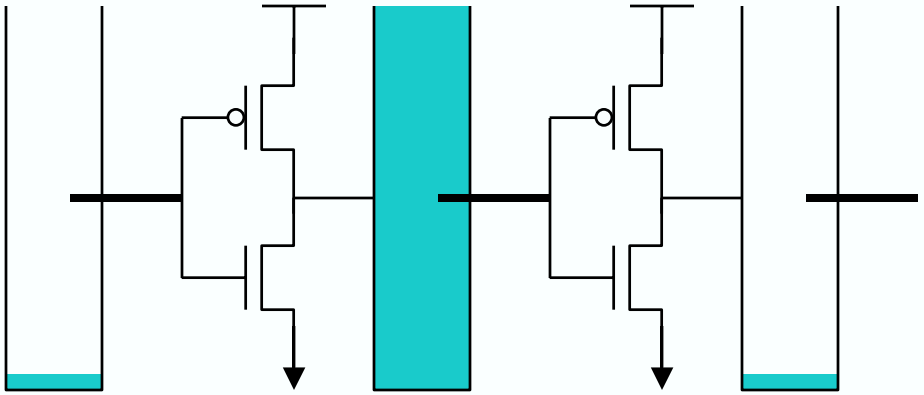
RC Switch Model





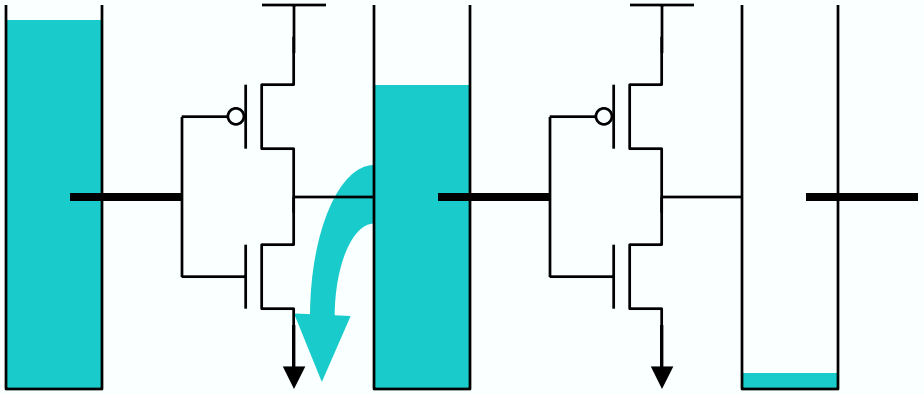
Signal Propagation (1)

t < 0
Vin = 0



Vout = 0

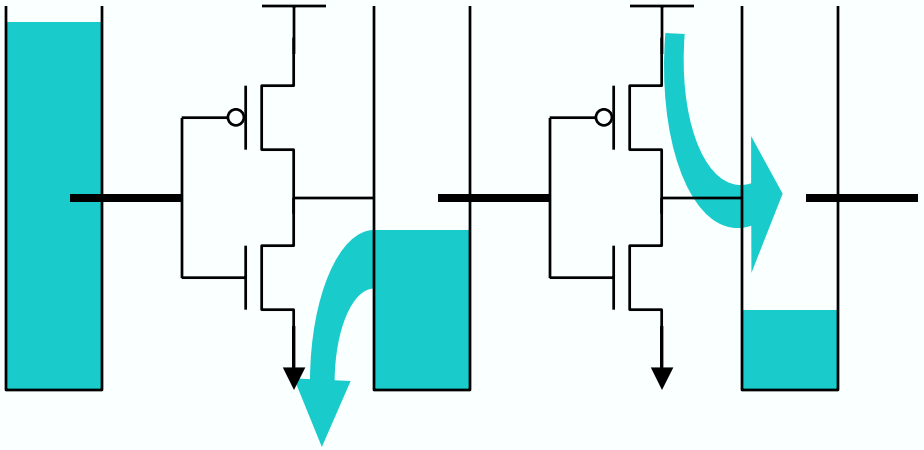
t = 0
Vin = 1



Vout = 0

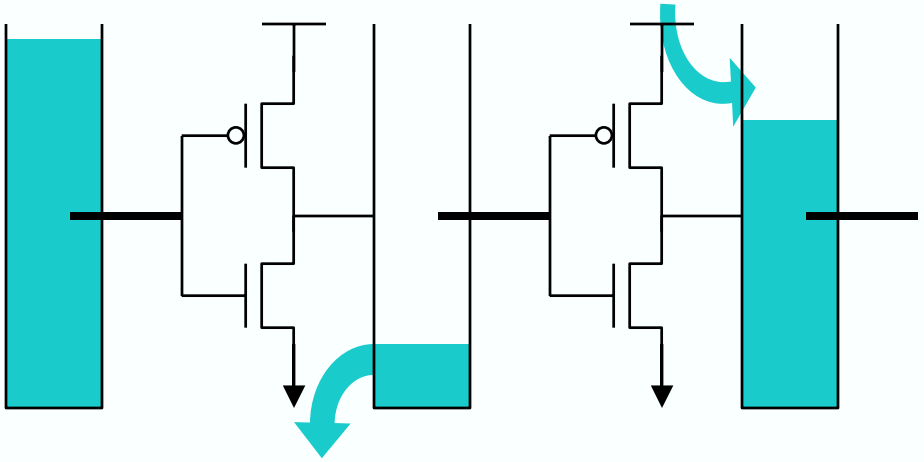
Signal Propagation (2)

t = 1
Vin = 0



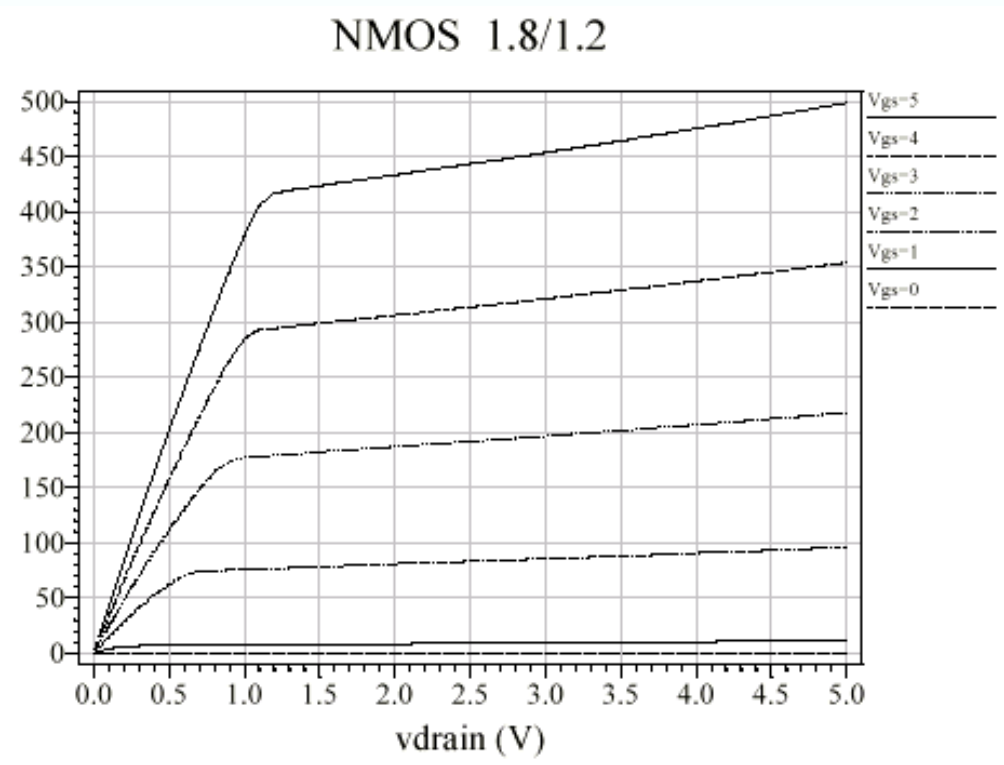
Vout = 0

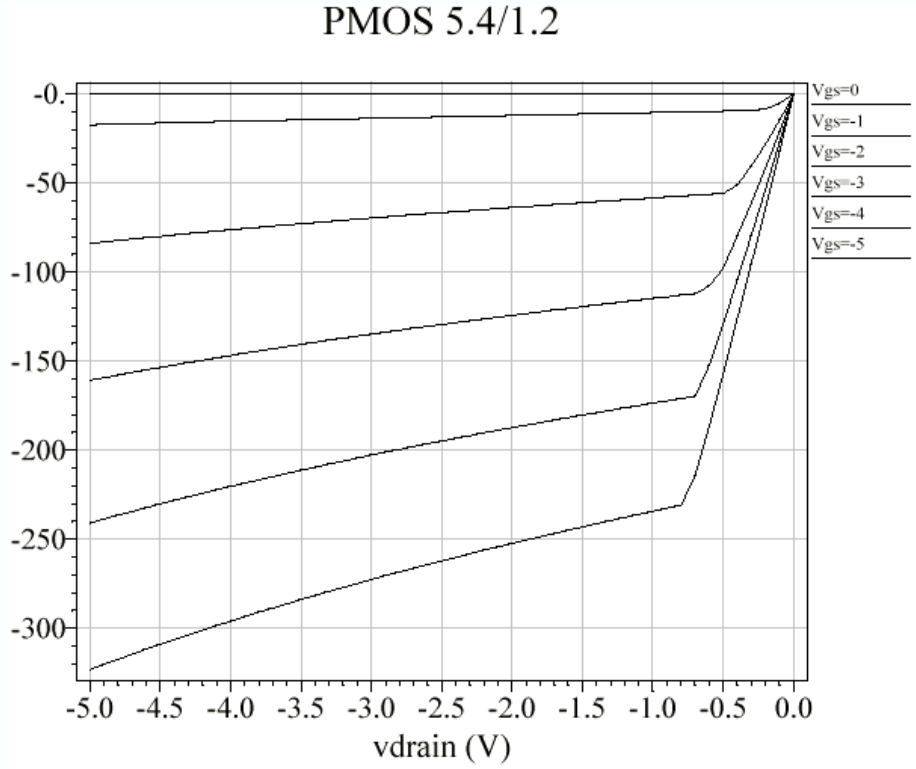
t = 2
Vin = 1



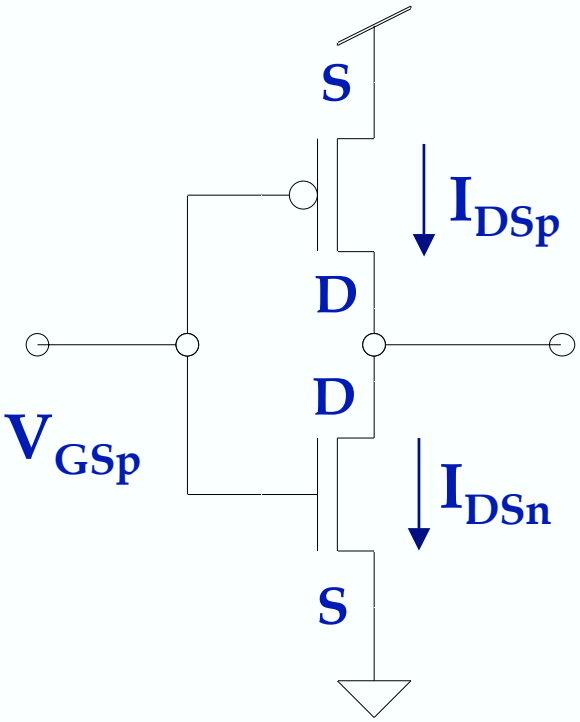
Vout = 1

MOSFET IV Characteristics





CMOS Inverter



$V_{in} = V_{GSn}$
$= V_{DD} + V_{GSp}$

I_{DSp}

I_{DSn}

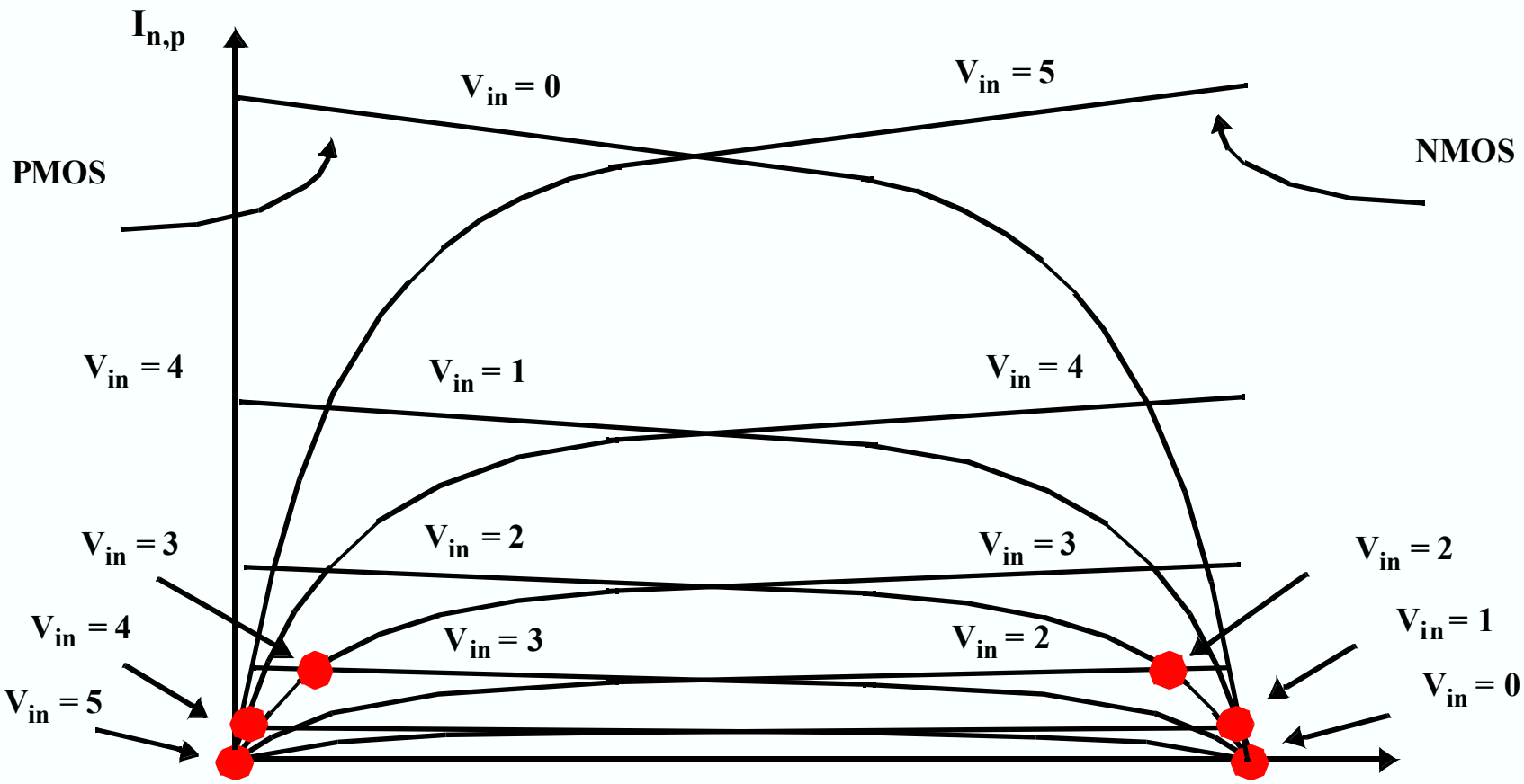
V_{out}

$I_{DSp} = - I_{DSn}$

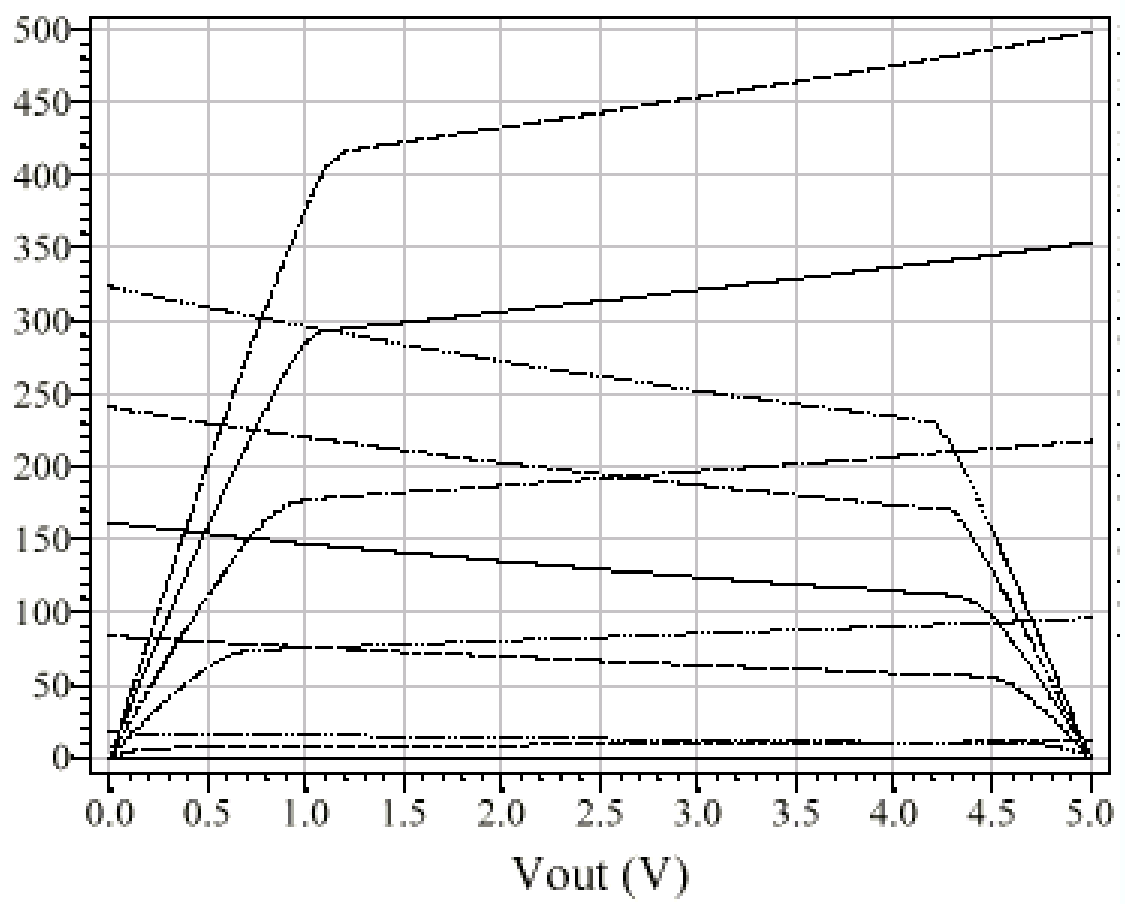
$V_{DSp} = V_{out} - V_{DD}$

$V_{DSn} = V_{out}$

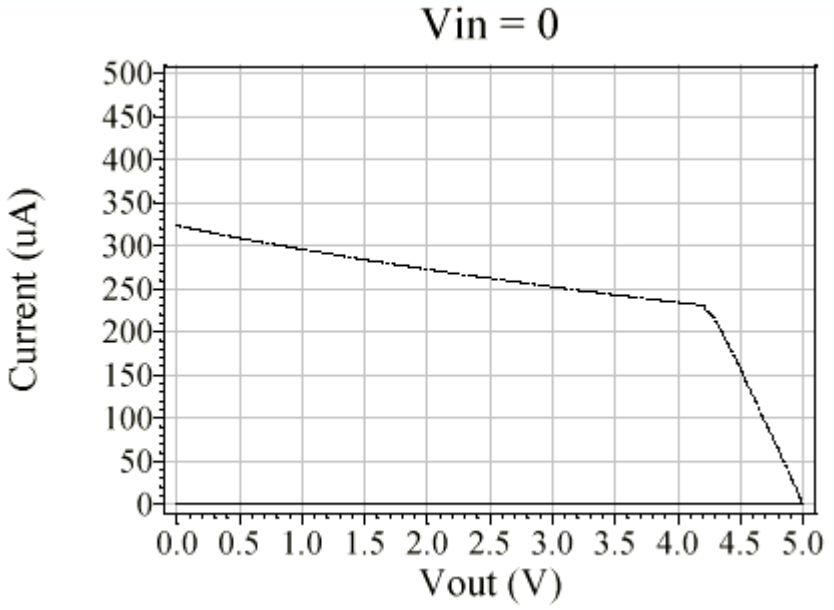
CMOS Inverter Load Characteristics

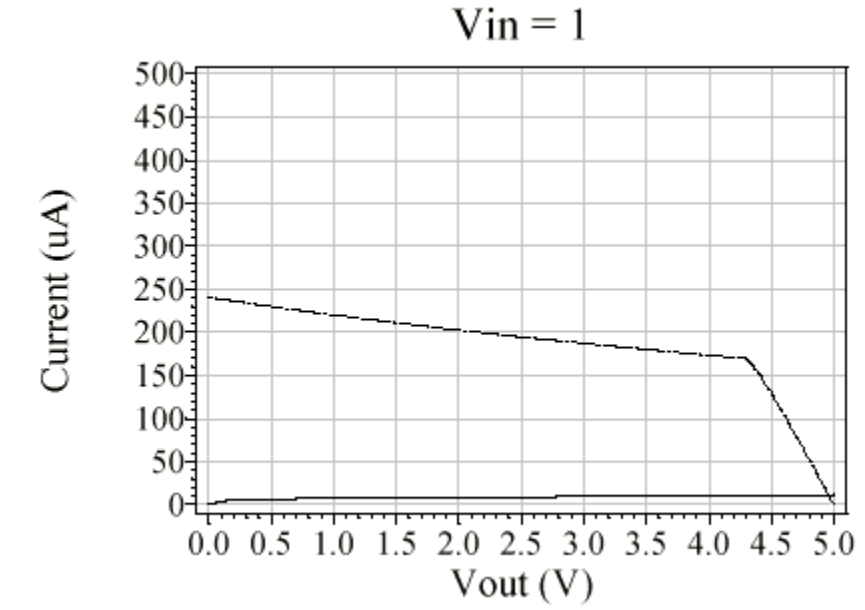


CMOS "Load Lines"

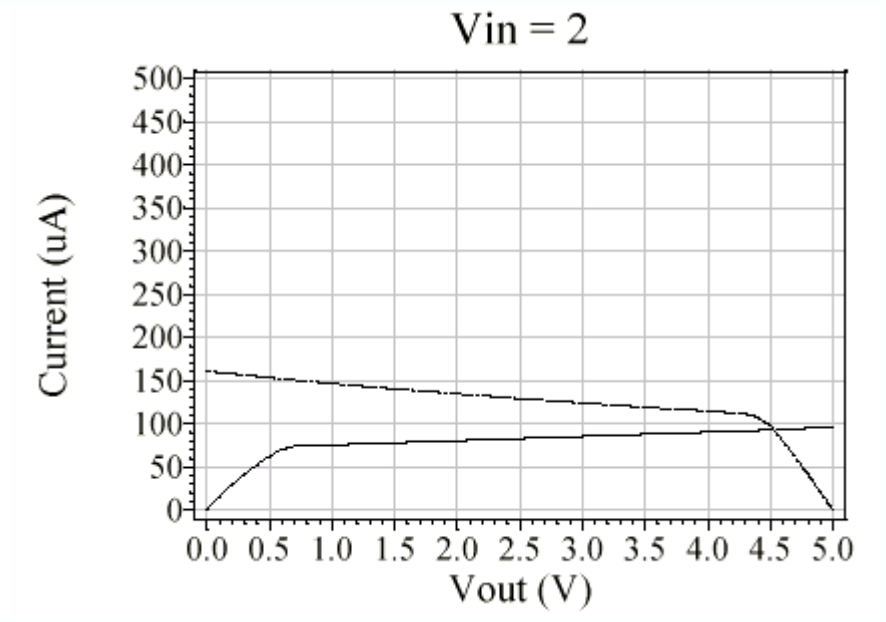


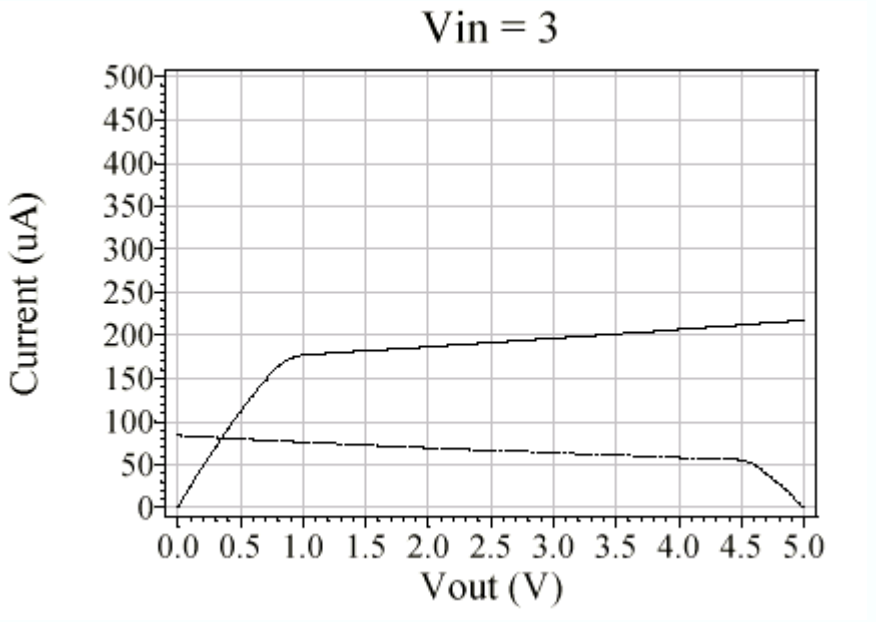
Finding CMOS VTC--1



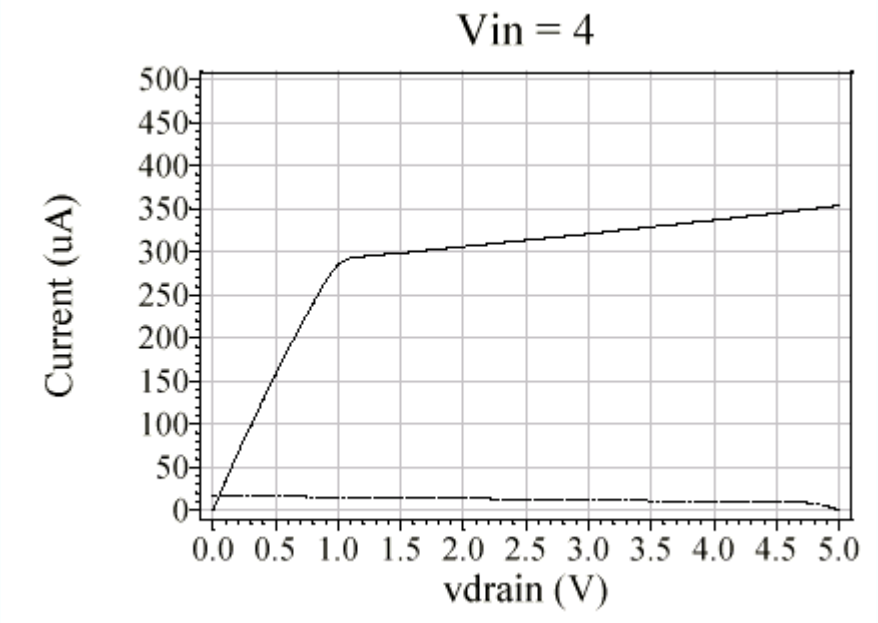


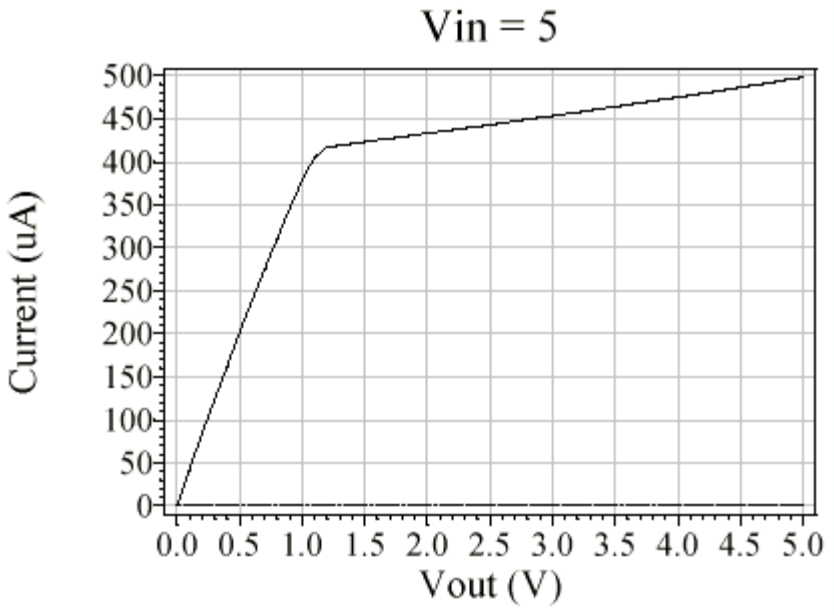
Finding CMOS VTC--2



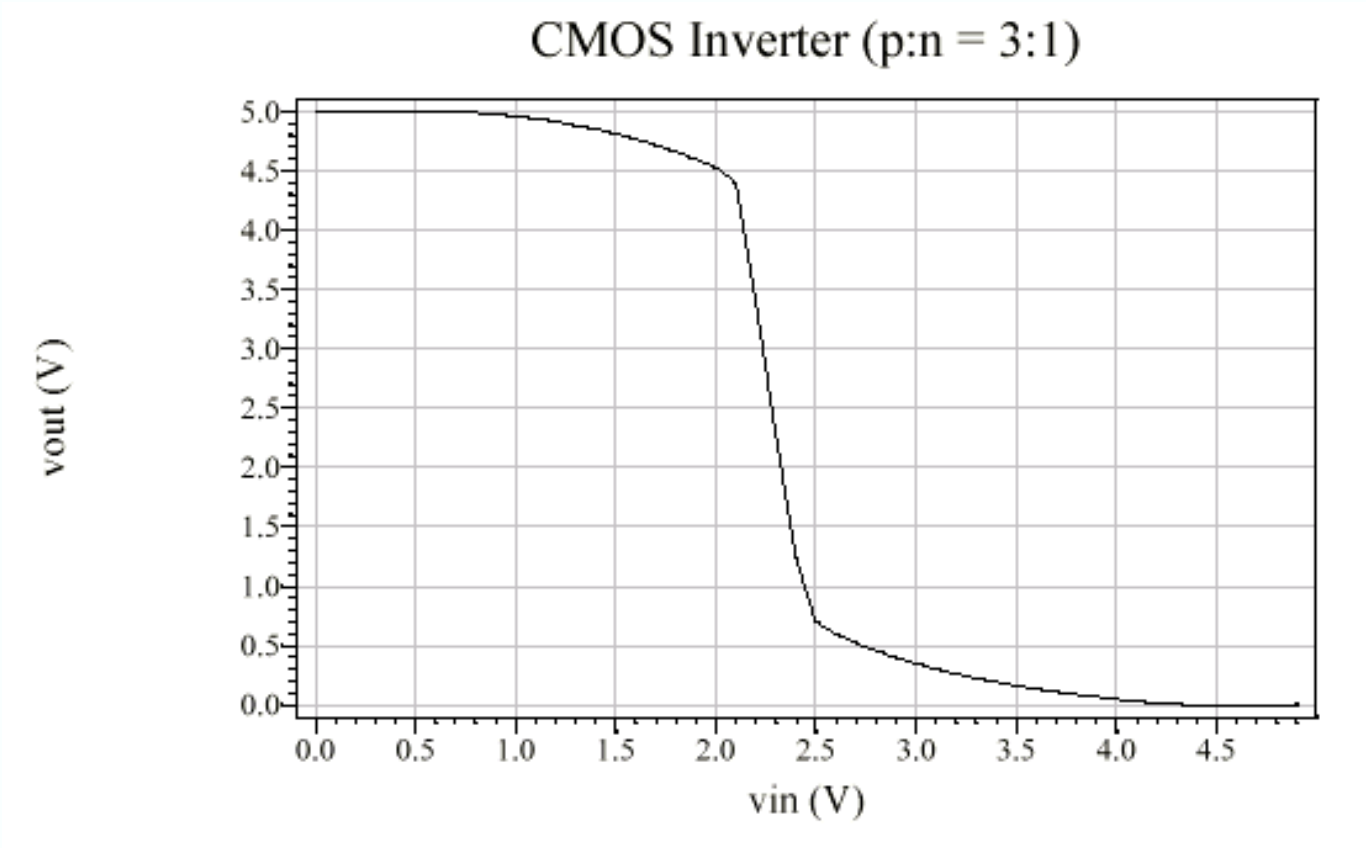


Finding CMOS VTC--3

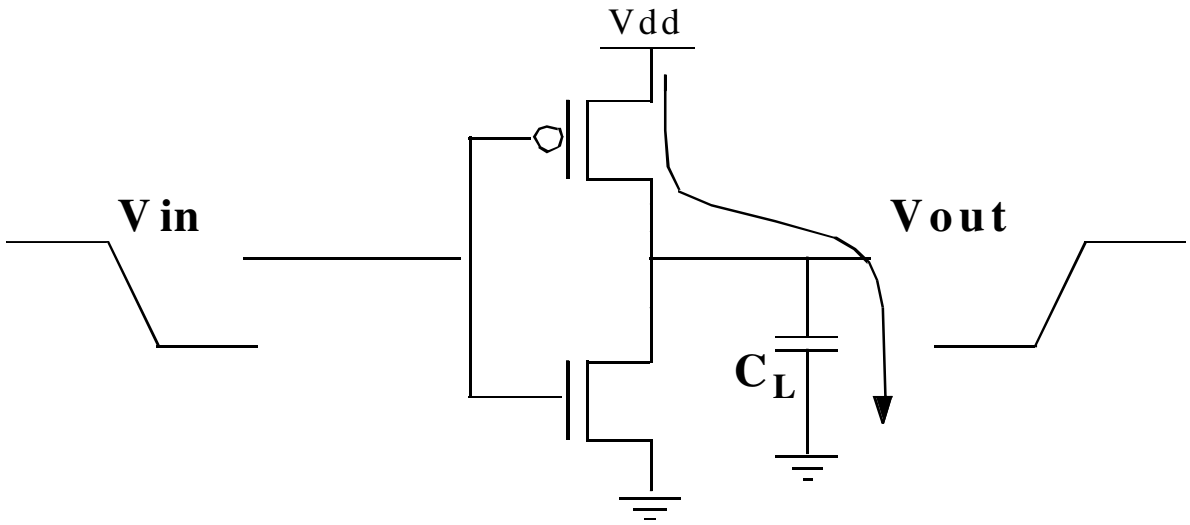




CMOS VTC--Spice Results



Dynamic Power Consumption

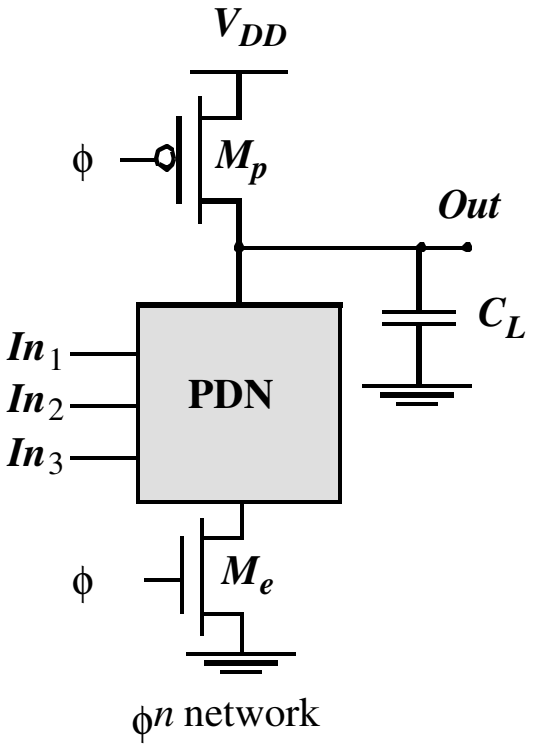


$$\text{Energy/transition} = C_L * V_{dd}^2$$

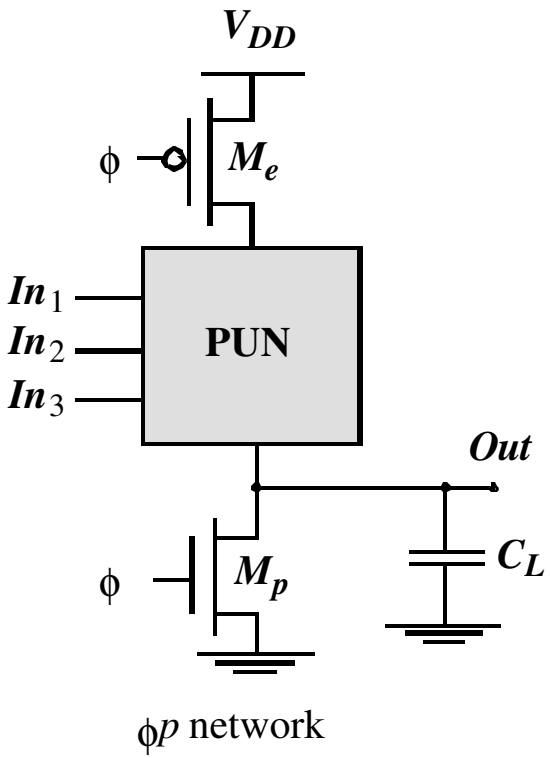
$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2 * f$$

- Not a function of transistor sizes!
- Need to reduce C_L, V_{dd}, and f to reduce power.

Dynamic Logic



ϕn network



ϕp network

2 phase operation:

- Precharge
- Evaluatio

