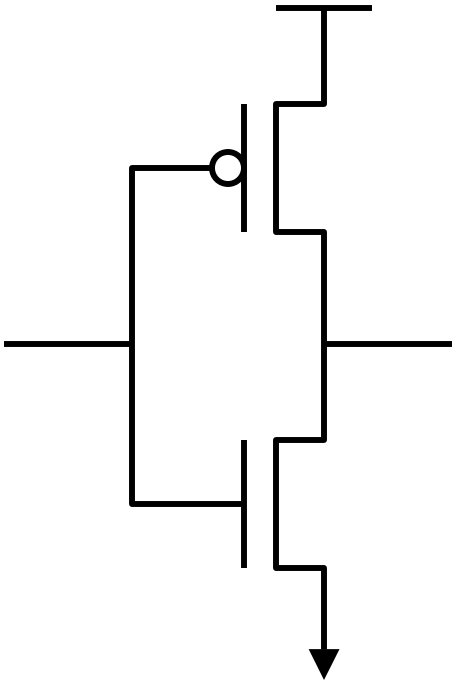
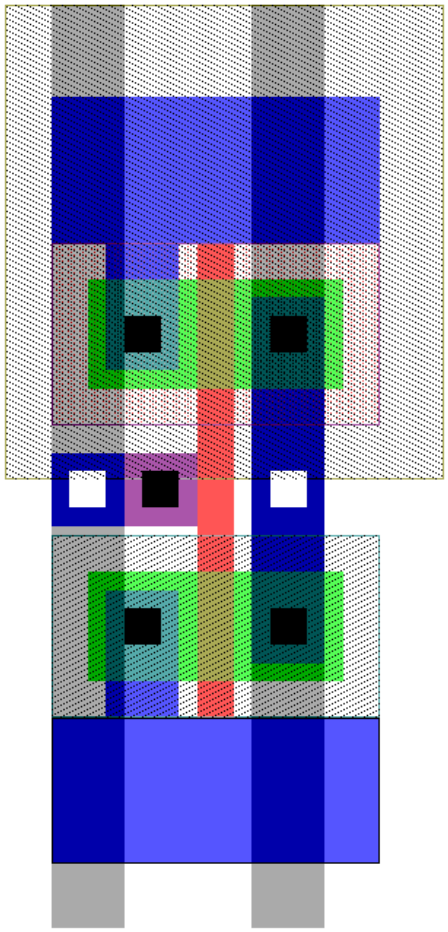
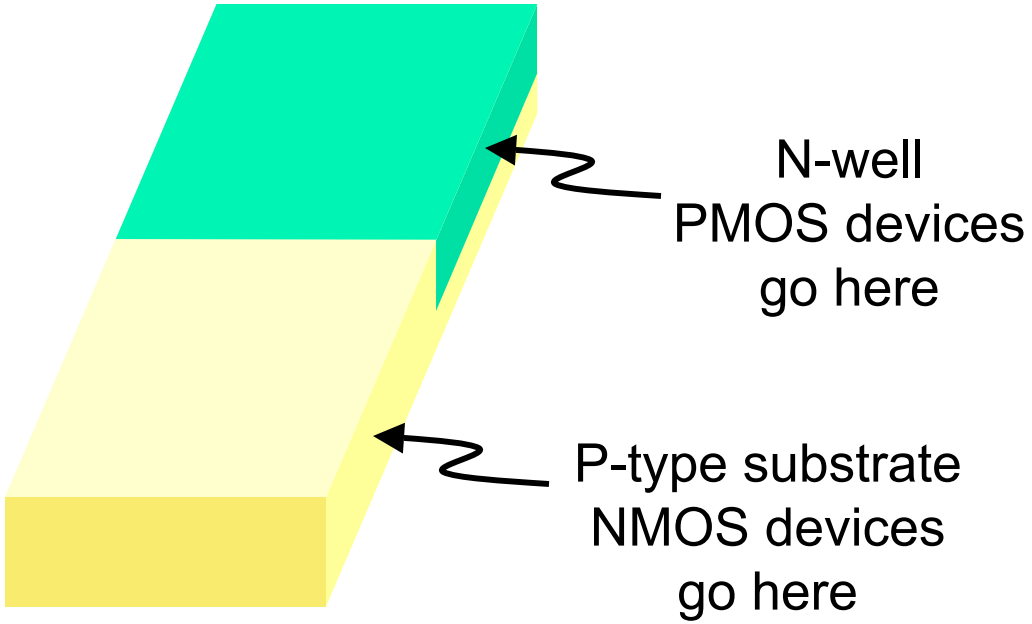
CMOS Fabrication Process
and
MOSIS SCMOS Mask Layers

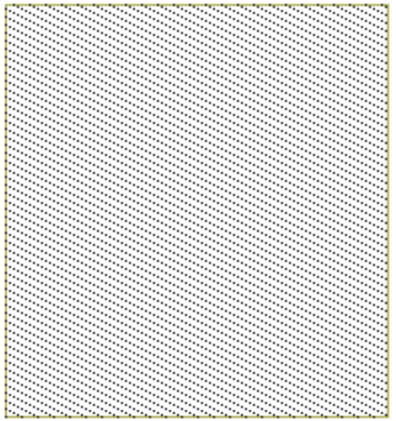
CMOS Inverter





P-Type Substrate and N-Well



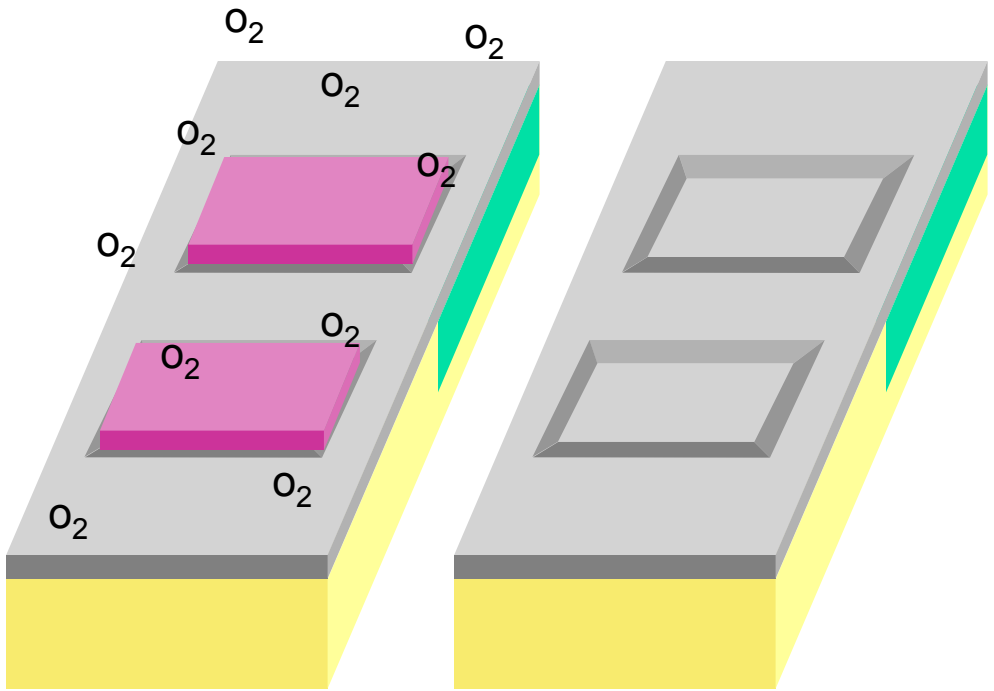


N-well mask

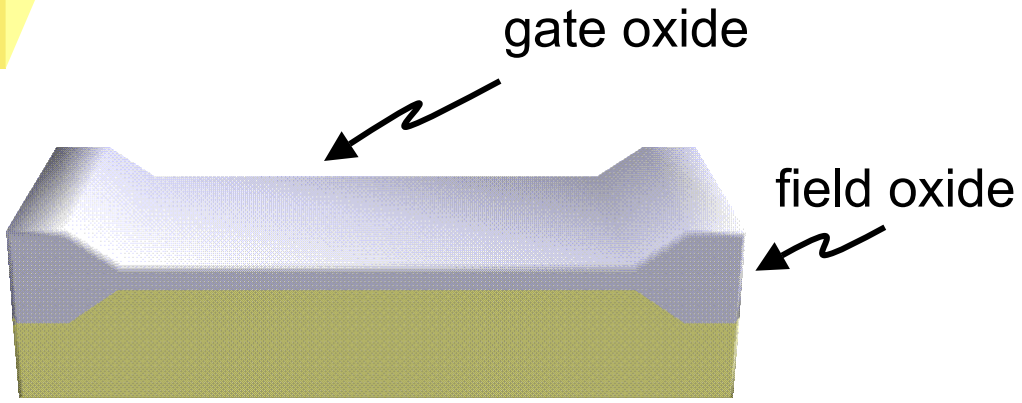
Active Area

active mask defines p-type and n-type mosfet locations (drain-gate-source)

Field Oxide Growth

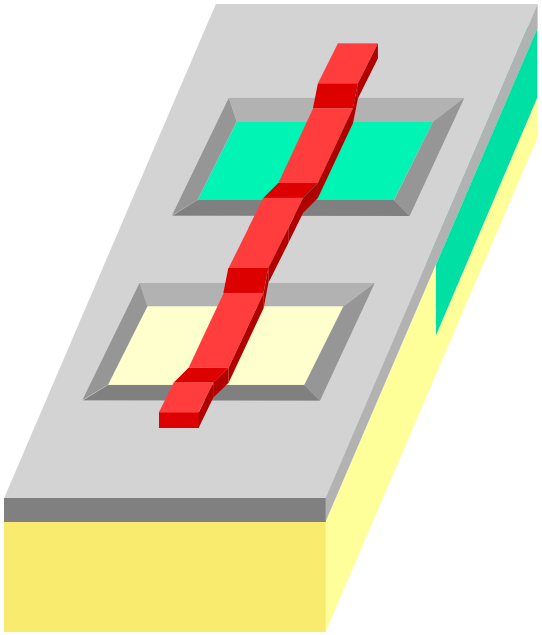


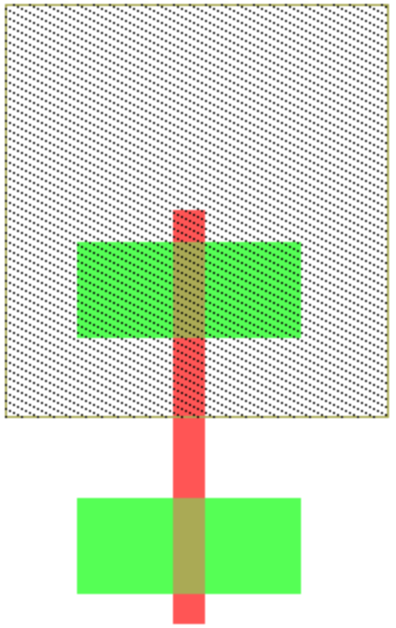
- Thick field oxide electrically isolates transistors
- Nitride prevents field oxide growth
- Thin gate oxide grown after nitride removed



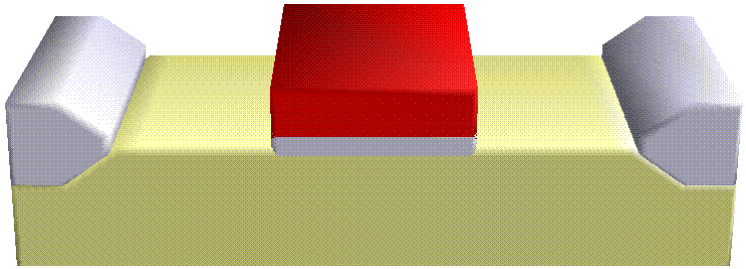
- SiO_2 formation consumes Si
- Si-SiO_2 interface below original Si surface

Polysilicon Gate

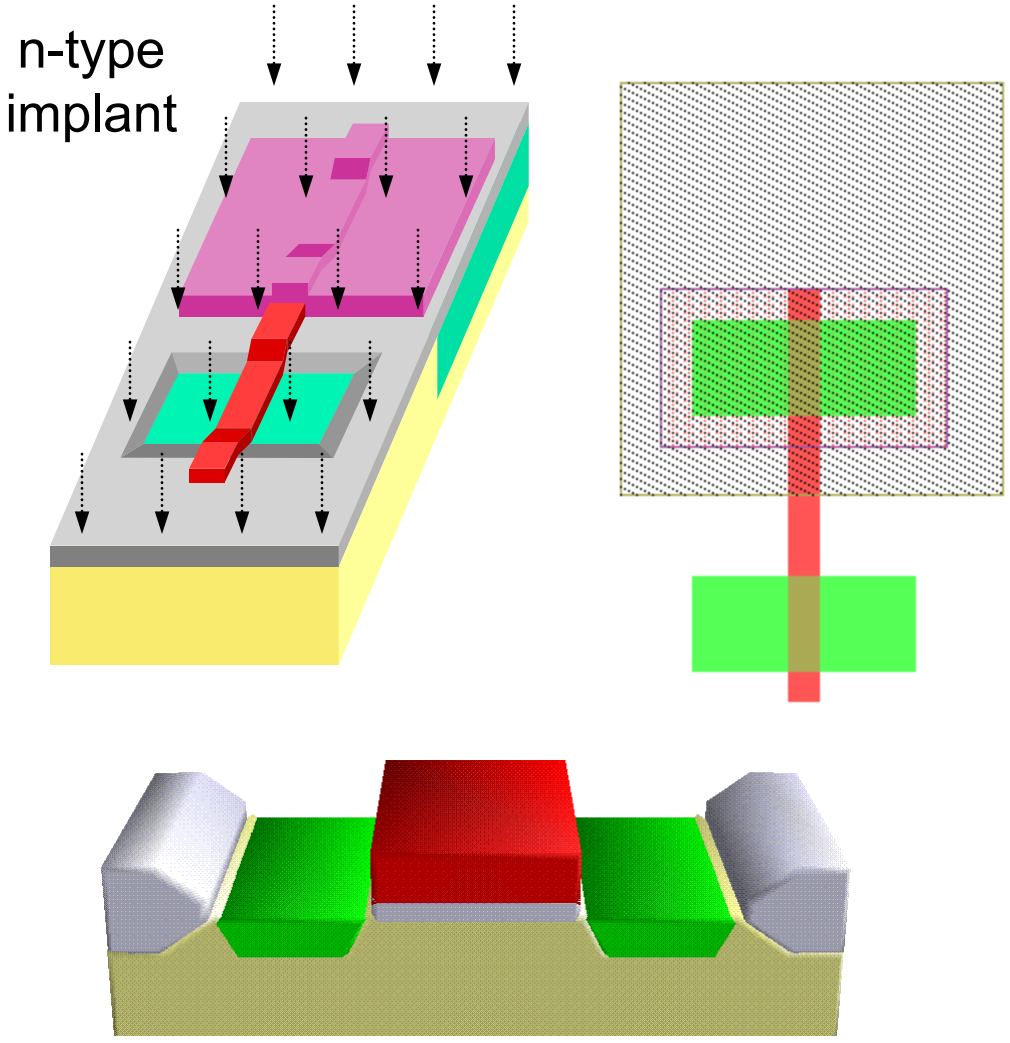




poly mask
added to layout

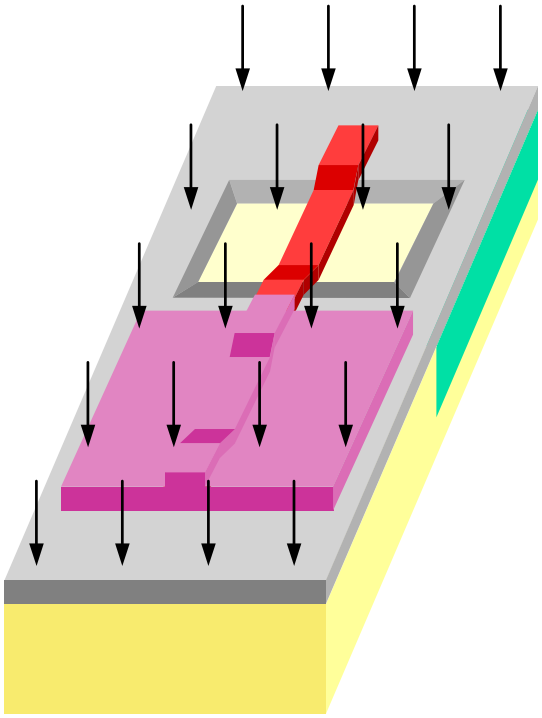


P-Select Mask and N-Type Source/Drain Implant

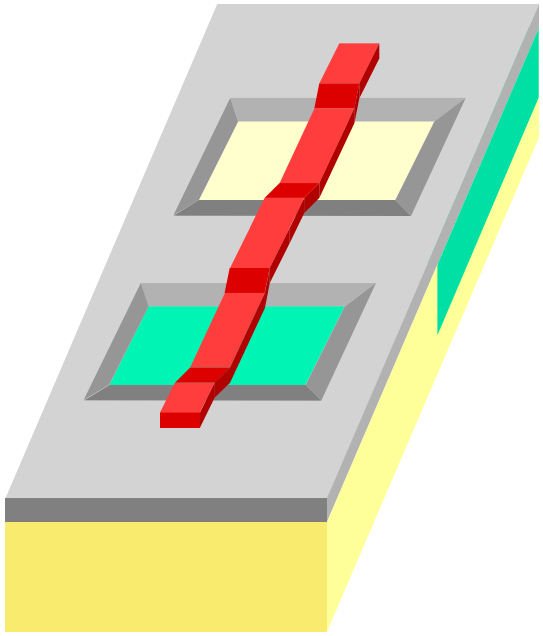


- p-select covers p-type source/drain regions
- select mask must overlap active areas
- n-type ion implant creates n-type source/drain regions
- high temperature anneal repairs silicon lattice and causes diffusion of implanted ions

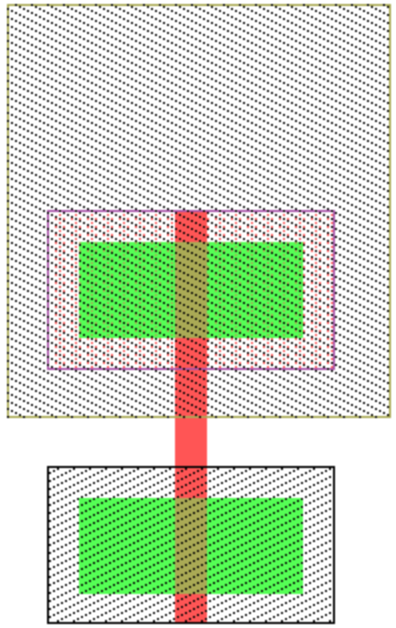
N-Select Mask and P-Type Source/Drain Implant



p-type implant

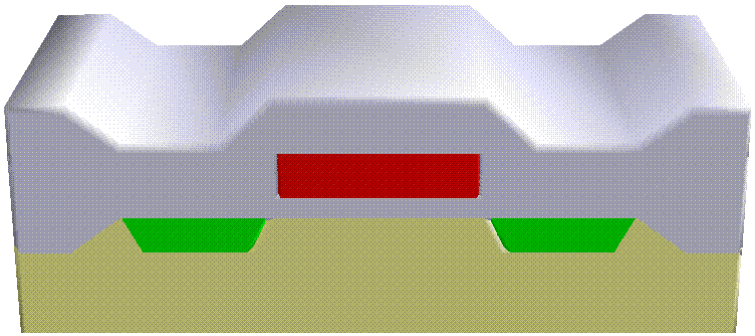


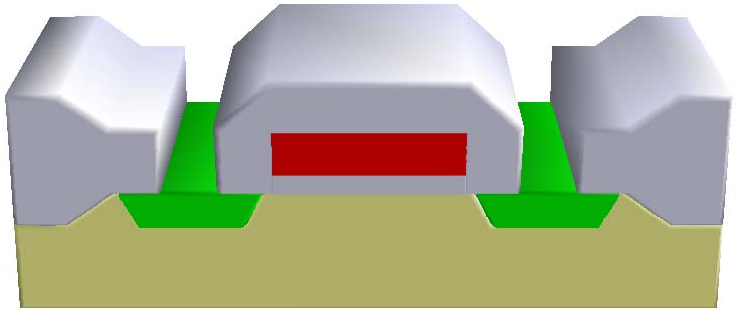
finished mosfets

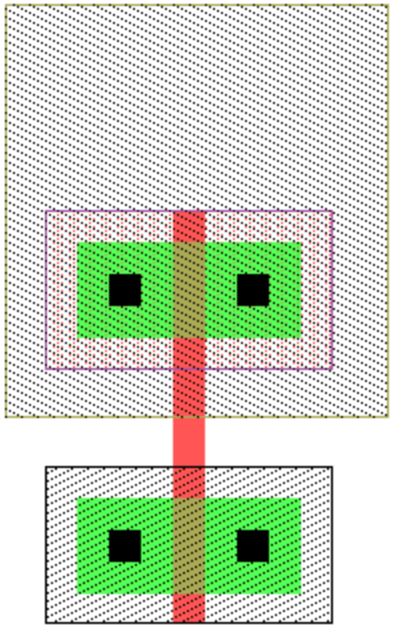


both select masks added

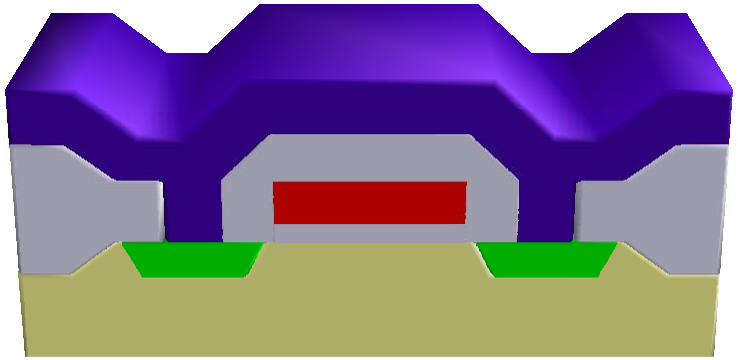
Contact Cuts



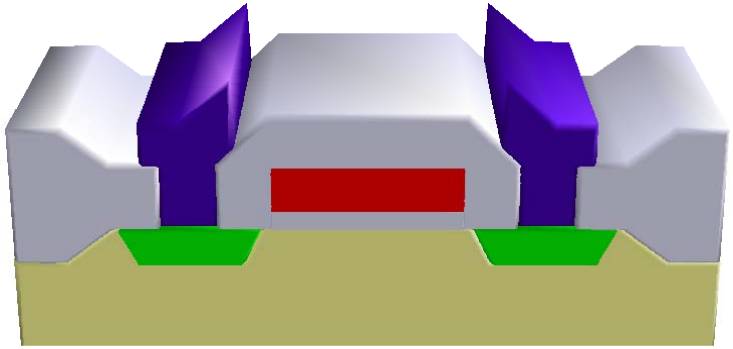


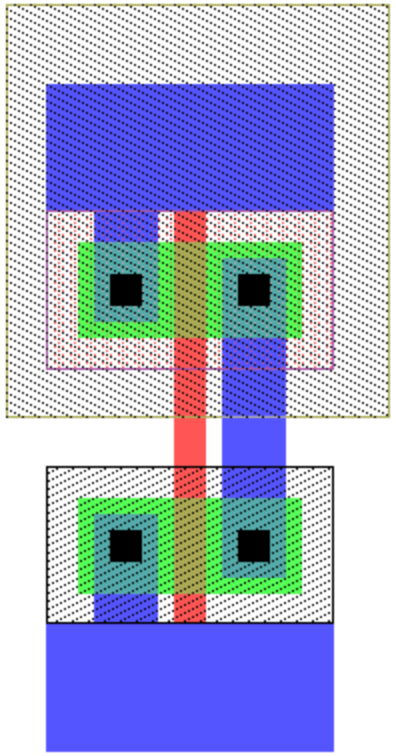


Metal 1

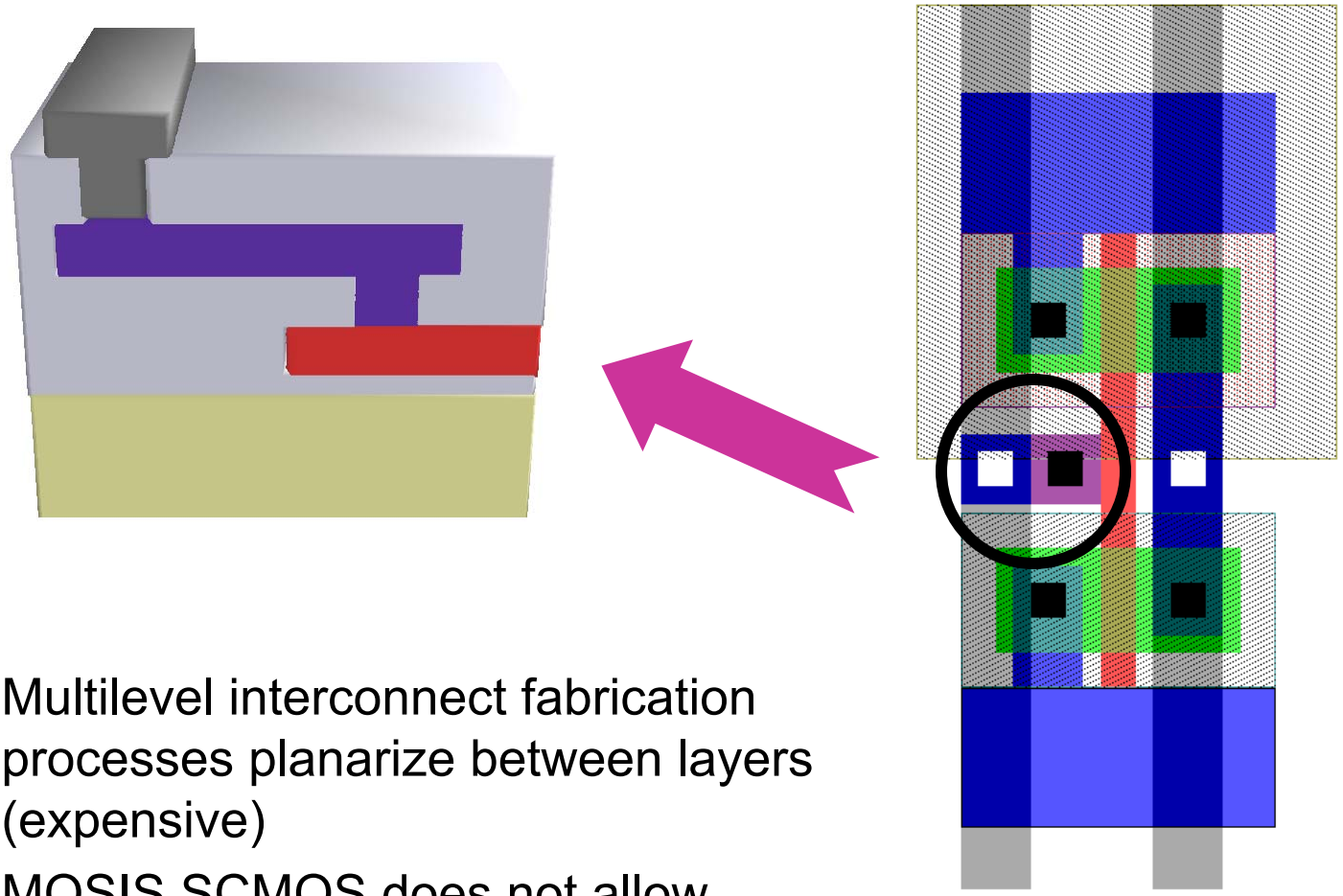


non-planar surface





Via 1 and Metal 2



- Multilevel interconnect fabrication processes planarize between layers (expensive)
- MOSIS SCMOS does not allow stacked vias