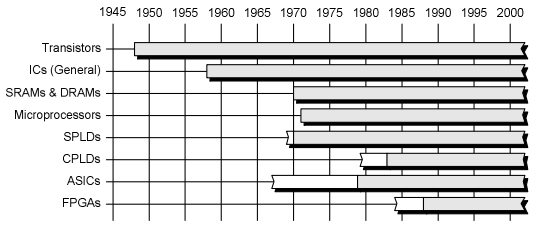
Origin of FPGAs

ADAPTED FROM:

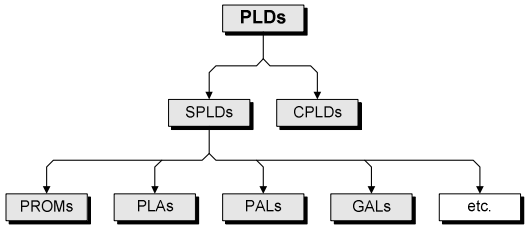
The Design Warrior's Guide to FPGAs
Devices, Tools, and Flows. ISBN 0750676043

(www.mentor.com)

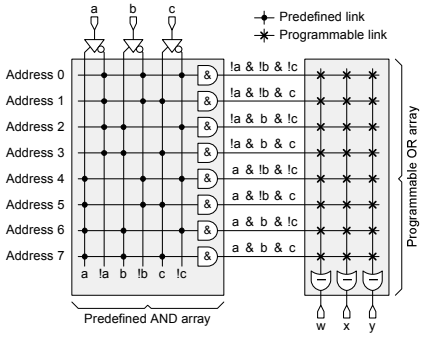
Technology timeline



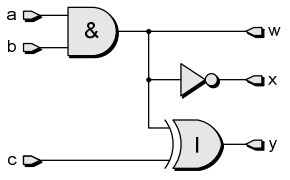
Programmable Logic Devices



Unprogrammed PROM

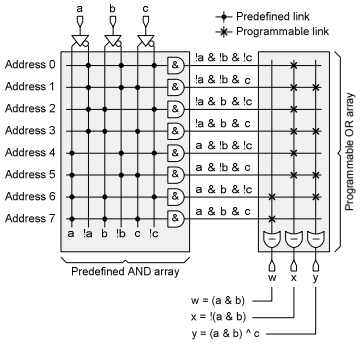


Some Combinational Logic

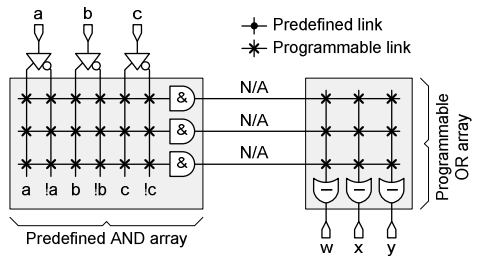


a	b	c	w	x	y
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	0	0

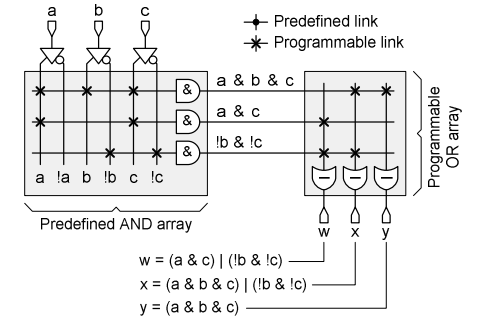
Programmed PROM



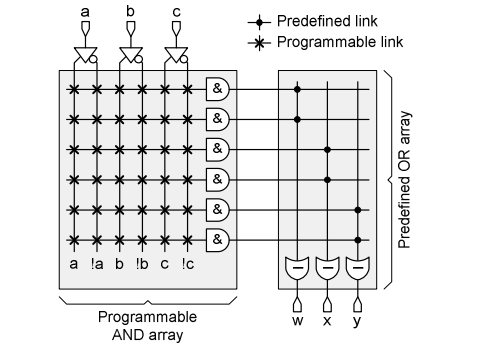
Unprogrammed PLA



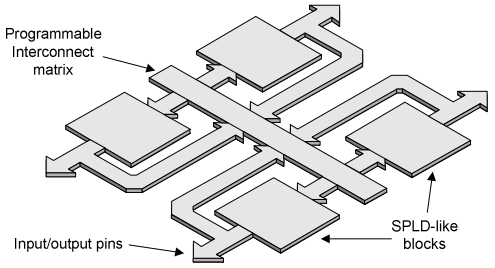
Programmed PLA



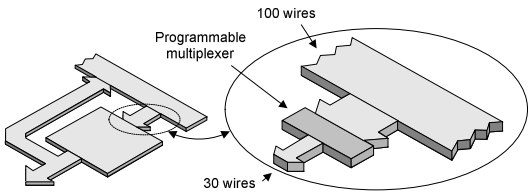
Unprogrammed PAL



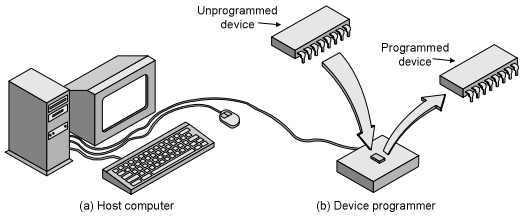
Generic CPLD Structure



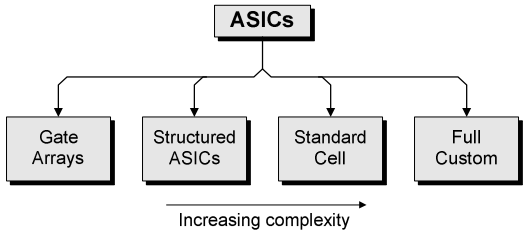
Using Programmable Multiplexers



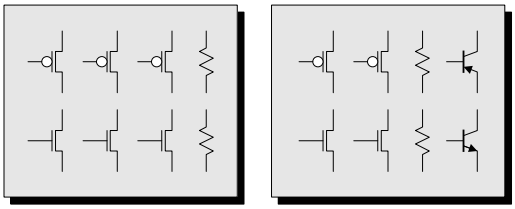
Programming a Physical PLD



Different Types of ASICs

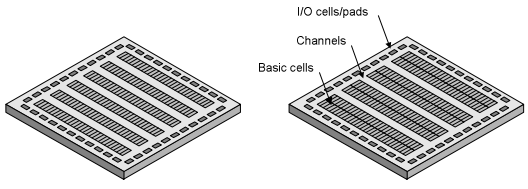


Examples of simple gate array basic cells



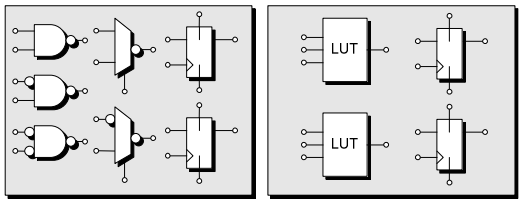
(a) Pure CMOS basic cell (b) BiCMOS basic cell

Channeled gate array architectures



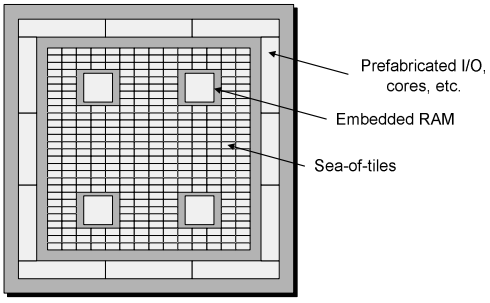
(a) Single-column arrays (b) Dual-column arrays

Structured ASIC tiles

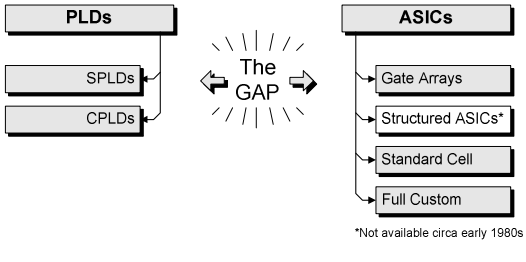


(a) Gate, mux, and flop-based (b) LUT and flop-based

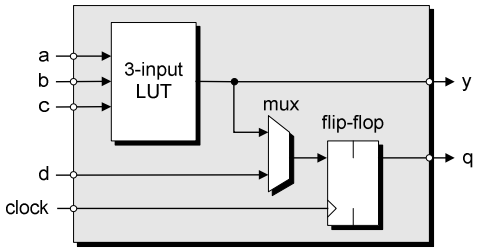
Generic structured ASIC



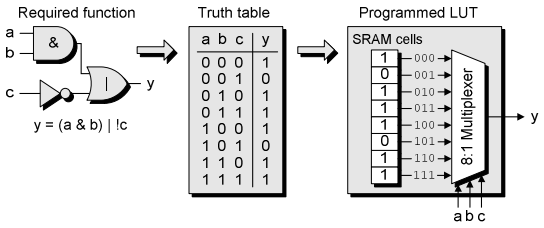
The Gap-- FPGAs



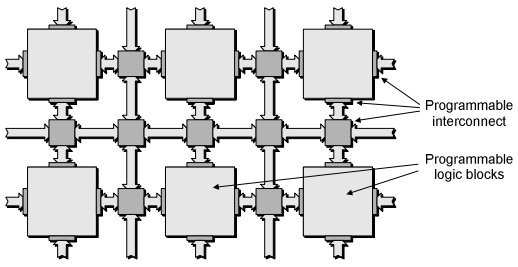
Simple Logic Block



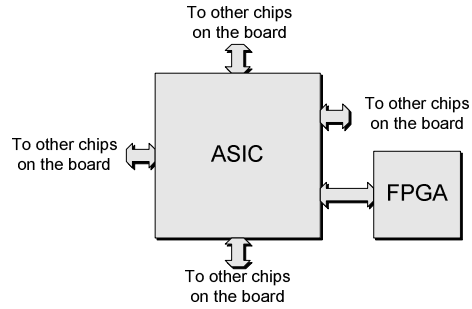
Configuring a LUT



Simple generic FPGA architecture



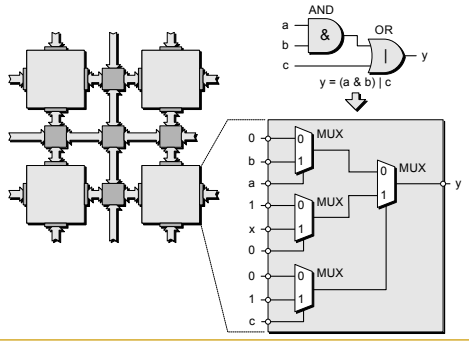
FPGA augmenting an ASIC



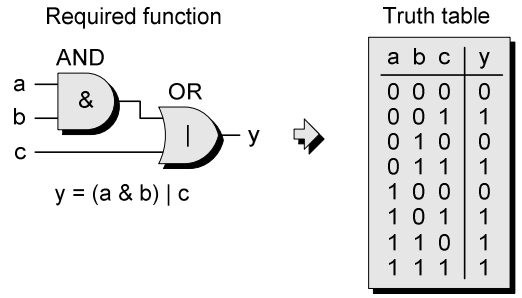
Summary of Programming Technologies

Feature	SRAM	Antifuse	E2PROM / FLASH
Technology node	State-of-the-art	One or more generations behind	One or more generations behind
Reprogrammable	Yes (in system)	No	Yes (in-system or offline)
Reprogramming speed (inc. erasing)	Fast	----	3x slower than SRAM
Volatile (must be programmed on power-up)	Yes	No	No (but can be if required)
Requires external configuration file	Yes	No	No
Good for prototyping	Yes (very good)	No	Yes (reasonable)
Instant-on	No	Yes	Yes
IP Security	Acceptable (especially when using bitstream encryption)	Very Good	Very Good
Size of configuration cell	Large (six transistors)	Very small	Medium-small (two transistors)
Power consumption	Medium	Low	Medium
Rad Hard	No	Yes	Not really

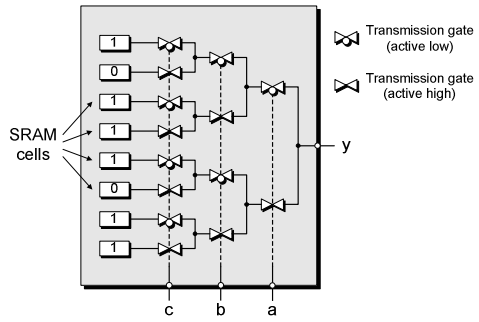
Mux-based logic block



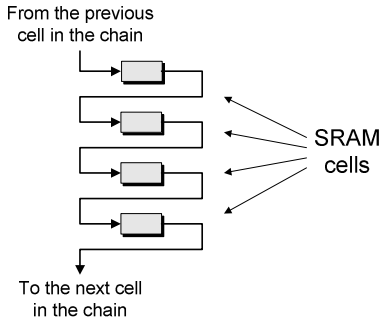
Function and Table



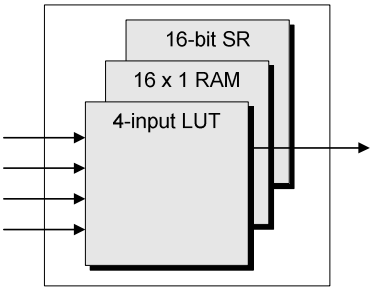
Transmission-based LUT



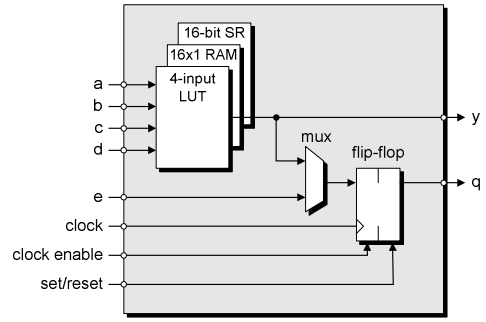
Configuration cells linked in a chain



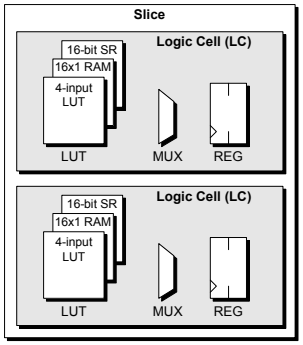
A Multifaceted LUT



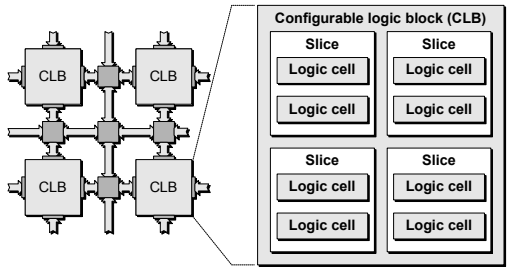
Xilinx Logic Cell



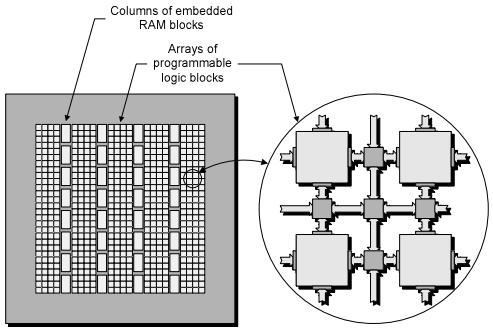
Xilinx slice



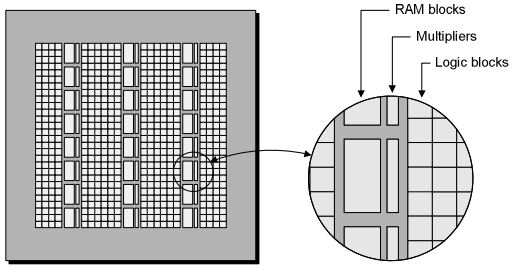
Xilinx CLB



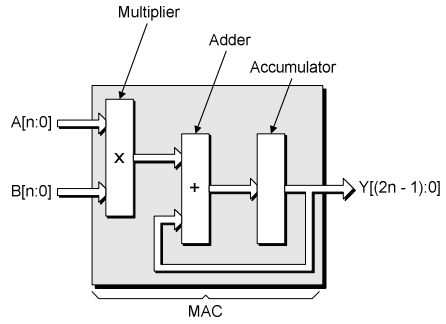
Embedded RAM Blocks



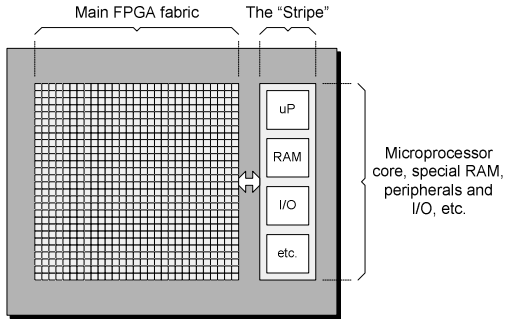
Embedded Multipliers and RAM blocks



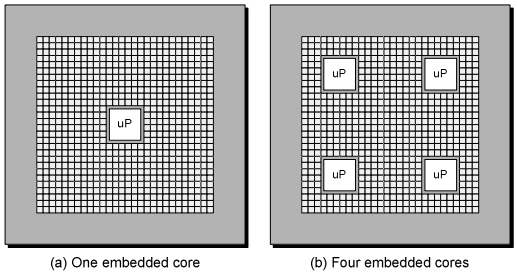
Multiplier-Accumulator



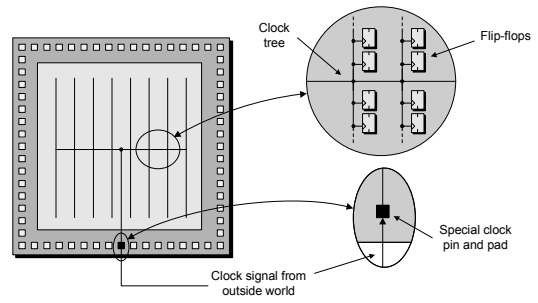
Embedded Microprocessor core



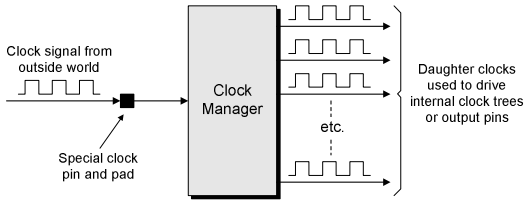
Multiple Cores



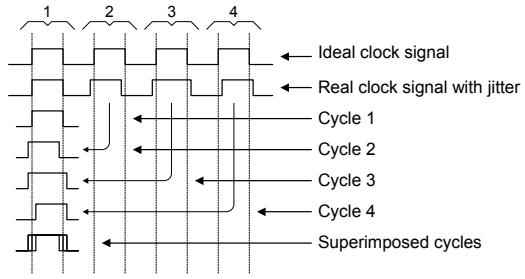
Simple Clock Tree



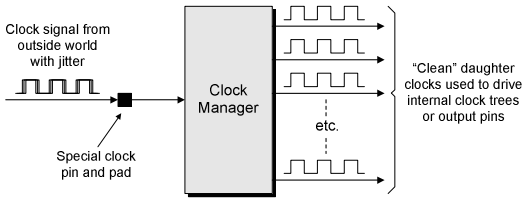
Managing Clocks



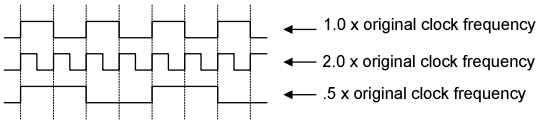
Jitter



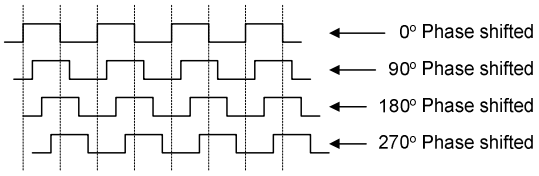
Jitter remover



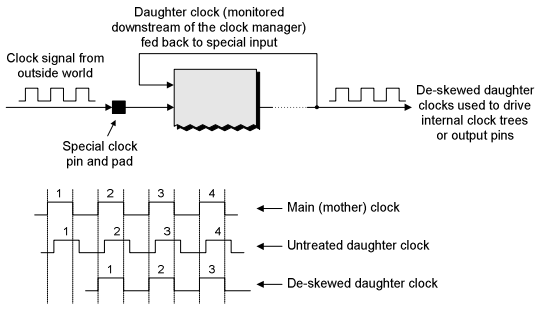
Frequency Synthesis



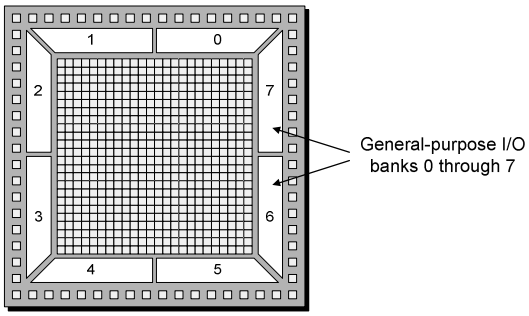
Phase-shifted Clocks



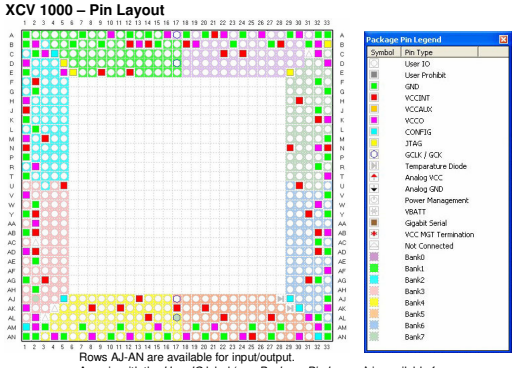
Deskewing



General-purpose IO banks



XCV 1000 – Pin Layout



Rows AJ-AN are available for input/output.
Any pin with the *User IO* label (see *Package Pin Legend*) is available for use.