# Introduction to Re-usable IP and MicroBlaze™ architecture
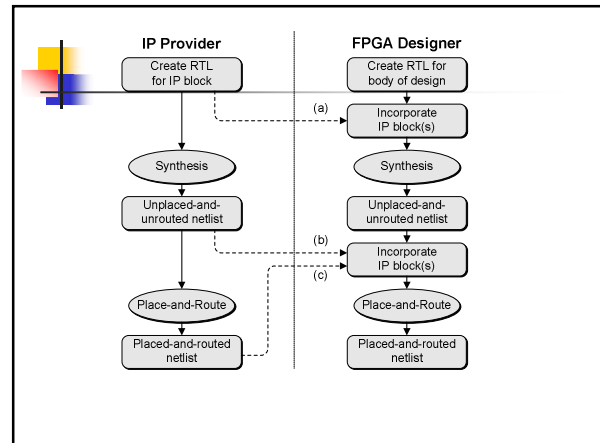
32-bit RISC soft processor core
for Xilinx FPGAs

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## Productivity Problem

- Designer = 100 gates/day, 10 lines tested-debugged verilog
- Design = 200,000 gates, optimum design team = 2
- Project = 1000 days, almost 3 years!
- Management expects project done in a year or less
- Result = Big Problem!

- Solutions?

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## Productivity Increase

- Bigger Design team
- Coffman's Law
- Individual designer must produce more code
- Each line of code represents more gates
- Reuse designs
  - Libraries
  - Reuse old projects
  - Buy IP (Intellectual Property)

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IP Provider — FPGA Designer flow:
Create RTL for IP block / Create RTL for body of design → (a) Incorporate IP block(s) → Synthesis → Unplaced-and-unrouted netlist → (b) (c) Incorporate IP block(s) → Place-and-Route → Placed-and-routed netlist

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## Structural Verilog

```
module xor_gate (out,a,b);
  input    a,b;
  output   out;
  wire     abar, bbar, t1, t2;
  not      inva (abar,a);
  not      invb (bbar,b);
  and      and1 (t1,abar,b);
  and      and2 (t2,bbar,a);
  or       or1 (out,t1,t2);
endmodule
```
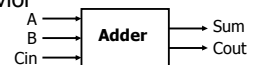
8 basic gates (keywords):
and, or, nand, nor
buf, not, xor, xnor



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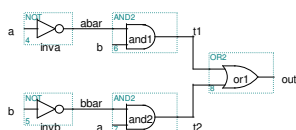
## Behavioral Verilog

- **Describe circuit behavior**
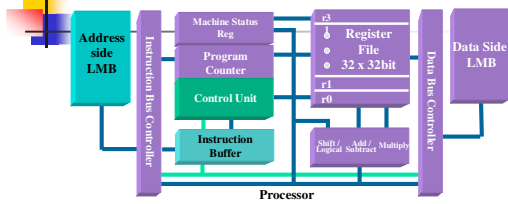  - Not implementation



```
module full_addr (Sum,Cout,A,B,Cin);
  input    A, B, Cin;
  output   Sum, Cout;
  assign   {Cout, Sum} = A + B + Cin;
endmodule
```

{Cout, Sum} is a concatenation
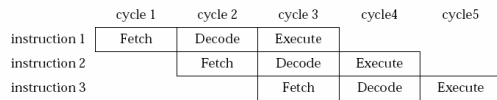
## What is MicroBlaze?



- It's a soft processor, around 900 LUTs
- RISC Architecture
- 32-bit, 32 x 32 general purpose registers
- Supported in Virtex/E/II/IIPro, Spartan-III/II/E

## MicroBlaze features

- Thirty-two 32-bit general purpose registers
- 32-bit instruction word with three operands and two addressing modes
- Separate 32-bit instruction and data buses that conform to IBM's OPB (On-chip Peripheral Bus) specification
- Separate 32-bit instruction and data buses with direct connection to on-chip block RAM through a LMB (Local Memory Bus)
- 32-bit address bus
- Single issue pipeline
- Instruction and data cache
- Hardware debug logic
- FSL (Fast Simplex Link) support

## Instruction pipeline

|              | cycle 1 | cycle 2 | cycle 3 | cycle4  | cycle5  |
|--------------|---------|---------|---------|---------|---------|
| instruction 1 | Fetch   | Decode  | Execute |         |         |
| instruction 2 |         | Fetch   | Decode  | Execute |         |
| instruction 3 |         |         | Fetch   | Decode  | Execute |

## Big-Endian Data Type



```
struct {
    int a; /* 0x1112_1314 word */
    long long b; /* 0x2122_2324_2526_2728 double word */
    char *c; /* 0x3132_3334 word */
    char d[7]; /* 'A','B','C','D','E','F','G' array of bytes */
    short e; /* 0x5152 halfword */
    int f; /* 0x6162_6364 word */
} s;
```

## Embedded Development Kit (EDK)

- All encompassing design environment for Virtex-II Pro **PowerPC™** and **MicroBlaze** based embedded systems in Xilinx FPGAs
- Integration of mature FPGA and embedded tools with innovative IP generation and customization tools
- Delivery vehicle for Processor IP

## EDK System Design
### Comprehensive Tool Chain
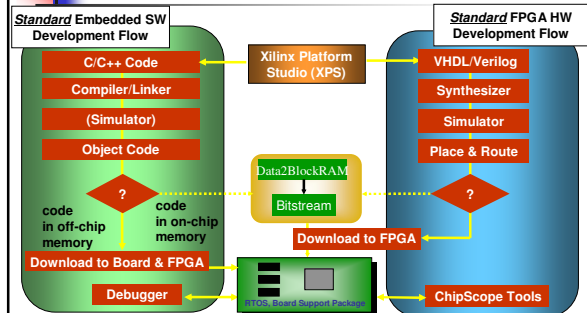
## More on MicroBlaze …

- Harvard Architecture
- Configurable instruction cache, data cache soon
- Non-intrusive JTAG debug
- Support for 2 buses:
  - LMB (Local Memory Bus) - 1 clock cycle latency, connects to BRAM
  - OPB (On-chip Peripheral Bus) - part of the IBM CoreConnect™ standard, connects to other peripheral "Portable" IP between PPC and MB
- Big endian, same as PowerPC PPC405
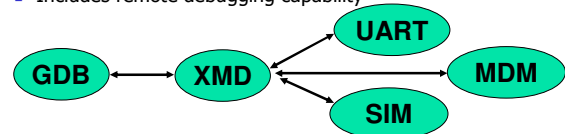
## MicroBlaze Interrupts and Exceptions

- Interrupt handling
  - 1 Interrupt port
    - 32+ interrupts and masking supported through interrupt controller(s)
- Exception handling
  - No exceptions generated in Virtex-II versions
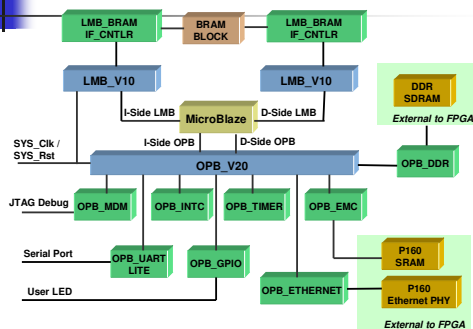  - One in Virtex/E and Spartan-II versions for MUL instruction

## Software Tools

- GNU tool chain
- GCC - GNU Compiler Collection
- GDB - The GNU debugger
  - Source code debugging
  - Debug either C or assembly code
- XMD - Xilinx Microprocessor Debug utility
  - Separate Process
  - Provides cycle accurate program execution data
  - Supported targets: simulator, hardware board

## Software - XMD

- Interfaces GDB to a "target"
- Allows hardware debug without a ROM monitor or reduces debug logic by using xmd-stub (ROM monitor)
- Offers a variety of simulation targets
  - Cycle accurate simulator
  - Real hardware board interface via UART or MDM
- Includes remote debugging capability

GDB ↔ XMD ↔ UART
XMD ↔ MDM
XMD ↔ SIM

## Example MicroBlaze System

LMB_BRAM IF_CNTLR   BRAM BLOCK   LMB_BRAM IF_CNTLR
LMB_V10   LMB_V10   DDR SDRAM — External to FPGA
I-Side LMB   MicroBlaze   D-Side LMB
SYS_Clk / SYS_Rst   I-Side OPB   D-Side OPB
OPB_V20   OPB_DDR
JTAG Debug   OPB_MDM   OPB_INTC   OPB_TIMER   OPB_EMC
Serial Port   OPB_UART LITE   OPB_GPIO   P160 SRAM
User LED   OPB_ETHERNET   P160 Ethernet PHY
External to FPGA

## Processor IP (HW/SW)

**Infrastructure (includes Device Drivers)**
- MicroBlaze CPU
- LMB2OPB Bridge
- PLB Arbiter & Bus Structure (PLB_V34)
- OPB Arbiter & Bus Structure (OPB_V20)
- DCR Bus Structure (DCR_V29)
- PLB2OPB Bridge
- OPB2PLB Bridge
- OPB2OPB Bridge - Lite
- OPB2DCR Bridge
- System Reset Module
- BSP Generator (SW only)
- ML3 VxWorks BSP (SW only)
- Memory Test Utility (SW only)

**OPB IPIF Modules (includes Device Drivers)**
- PLB IPIF
  - OPB IPIF-Slave Attachment
  - OPB IPIF-Master Attachment
  - IPIF-Address Decode
  - IPIF-Interrupt Control
  - IPIF-Read Packet FIFOs
  - IPIF-Write Packet FIFOs
  - IPIF-DMA
  - IPIF-Scatter Gather
  - IPIF-FIFOLink
- PLB IPIF
  - PLB IPIF-Slave Attachment
  - PLB IPIF-Master Attachment
  - IPIF-Address Decode
  - IPIF-Interrupt Control
  - IPIF-Read Packet FIFOs
  - IPIF-Write Packet FIFOs
  - IPIF-DMA
  - IPIF-Scatter Gather
  - IPIF-FIFOLink

## Processor IP (HW/SW)

**Memory Interfaces (includes Device Drivers & Memory Tests)**
- PLB EMC (Flash, SRAM, and ZBT)
- PLB BRAM Controller
- PLB DDR Controller
- PLB SDRAM Controller
- OPB EMC (Flash, SRAM, and ZBT)
- OPB BRAM Controller
- OPB DDR Controller
- OPB SDRAM Controller
- OPB SystemACE
- LMB BRAM Controller

**Peripherals (includes Device Drivers & RTOS Adapt. Layers)**
- OPB Single Channel HDLC Controller
- OPB<->PCI Full Bridge
- OPB 10/100M Ethernet
- OPB 10/100M Ethernet - Lite
- OPB ATM Utopia Level 2 Slave
- OPB ATM Utopia Level 2 Master

**Peripherals (continued)**
- OPB IIC Master & Slave
- OPB SPI Master & Slave
- OPB UART-16550
- OPB UART-16450
- OPB UART - Lite
- OPB JTAG UART
- OPB Interrupt Controller
- OPB TimeBase/Watch Dog Timer
- OPB Timer/Counter
- OPB GPIO
- PLB 1G Ethernet
- PLB RapidIO
- PLB UART-16550
- PLB UART-16450
- PLB ATM Utopia Level 2 Slave
- PLB ATM Utopia Level 2 Master
- PLB ATM Utopia Level 3 Slave
- PLB ATM Utopia Level 3 Master
- DCR Interrupt Controller

## System Infrastructure

- Hardware IP
  - Common PowerPC and MicroBlaze peripherals
  - Peripherals are common across bus types
  - Parameterize for optimal functionality, optimal FPGA usage
  - IP Interface (IPIF) provides common hardware blocks
- Software IP (Device Drivers)
  - Common across processors and operating systems
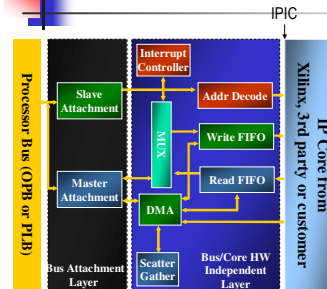
## The Benefits of Parameterization

Example: OPB Arbiter

| Parameter Values | | | | | Resources | $F_{MAX}$ |
|---|---|---|---|---|---|---|
| NUM_MASTERS | PROC_INTERFACE | DYNAM_PRIORITY | PARK | REG_GRANTS | LUTs | MHz |
| 1 | N | N | N | N | 11 | 295 |
| 2 | N | N | N | N | 18 | 223 |
| 4 | N | N | N | N | 34 | 193 |
| 4 | Y | N | N | N | 59 | 156 |
| 4 | N | Y | N | N | 54 | 169 |
| 4 | N | N | Y | N | 83 | 159 |
| 4 | N | N | N | Y | 34 | 201 |
| 4 | Y | Y | Y | Y | 146 | 145 |
| 8 | Y | Y | Y | Y | 388 | 112 |

Difference:
>4x in size
>30% in speed

- Significantly increases performance or saves area
- Only include what you need
- This can only be accomplished in a programmable system

## Full IP Interface (IPIF)

IPIC

Processor Bus (OPB or PLB)

Slave Attachment

Master Attachment

Interrupt Controller

MUX

Addr Decode

Write FIFO

Read FIFO

DMA

Scatter Gather

Bus Attachment Layer

Bus/Core HW Independent Layer

IP Core from Xilinx, 3rd party or customer

- Consists of 8 modules
  - Each module is selectable and parameterizable
- Automatically configures a core to the processor bus
  - Xilinx IP Cores
  - 3rd Party IP Cores
  - Customer proprietary cores and external devices
- OPB & PLB supported
  - Bus independent IP Cores and associated Device Drivers
- IPIF will be added to other LogiCOREs

## Buses and Arbiters

- PLB
  - Arbitration for up to 16 masters
  - 64-bit and 32-bit masters and slaves
  - IBM PLB compliant
- OPB
  - Includes arbiter with dynamic or fixed priorities and bus parking
  - Parameterized I/O for any number of masters or slaves
  - IBM OPB compliant
- DCR
  - Supports one master and multiple slaves
  - Daisy chain connections for the DCR data bus
  - Required OR function of the DCR slaves' acknowledge signal
- LMB
  - MicroBlaze single-master Local Memory Bus

## Bridges

- PLB to OPB
  - Decode up to 4 different address ranges
  - 32-bit or 64-bit PLB slave, 32-bit OPB master
  - Burst and non-burst transfers, cache-line transactions
- OPB to PLB
  - 64-bit PLB master, 32-bit OPB slave
  - Burst and non-burst transfers, cache-line transactions
  - BESR and BEAR
- OPB (slave) to DCR (master)
  - Memory mapped DCR control
- OPB to OPB
  - Allows further OPB partitioning

## More System Cores

- Processor System Reset
  - Asynchronous external reset input is synchronized with clock
  - Selectable active high or active low reset
  - DCM Locked input
  - Sequencing of reset signals coming out of reset:
    - First - bus structures come out of reset
    - Second - Peripheral(s) come out of reset 16 clocks later
    - Third - the CPU(s) come out of reset 16 clocks after the peripherals
- JTAG Controller
  - Wrapper for the JTAGPPC primitive.
  - Enables the PowerPC's debug port to be connected to the FPGA JTAG chain
- IPIF User Core Templates
  - Convenient way to add user core to OPB or PLB

## Timer / Counter

- Supports 32-bit OPB v2.0 bus interface
- Two programmable interval timers with interrupt, compare, and capture capabilities
- Programmable counter width
- One Pulse Width Modulation (PWM) output

## Watchdog Timer / Timebase

- Supports 32-bit bus interfaces
- Watchdog timer (WDT) with selectable timeout period and interrupt
- Two-phase WDT expiration scheme
- Configurable WDT enable: enable-once or enable-disable
- WDT Reset Status (was the last reset caused by the WDT?)
- One 32-bit free-running timebase counter with rollover interrupt

## Interrupt Controller

- Number of interrupt inputs is configurable up to the width of the data bus width
- Interrupt controllers can be easily cascaded to provide additional interrupt inputs
- Master Enable Register for disabling the interrupt request output
- Each input is configurable for edge or level sensitivity
  - rising or falling, active high or active low
- Output interrupt request pin is configurable for edge or level generation

## UART 16550 / 16450 / Lite

- Register compatible with industry standard 16550/16450
- 5, 6, 7 or 8 bits per character
- Odd, even or no parity detection and generation
- 1, 1.5 or 2 stop bit detection and generation
- Internal baud rate generator and separate RX clock input
- Modem control functions
- Prioritized transmit, receive, line status & modem control interrupts
- Internal loop back diagnostic functionality
- Independent 16 word transmit and receive FIFOs

## IIC

- 2-wire (SDA and SCL) serial interface
- Master/Slave protocol
- Multi-master operation with collision detection and arbitration
- Bus busy detection
- Fast Mode 400 KHz or Standard Mode 100 KHz operation
- 7 Bit, 10 Bit, and General Call addressing
- Transmit and Receive FIFOs - 16 bytes deep
- Bus throttling

## SPI

- 4-wire serial interface (MOSI, MISO, SCK, and SS)
- Master or slave modes supported
- Multi-master environment supported (requires tri-state drivers and software arbitration for possible conflict)
- Multi-slave environment supported (requires additional decoding and slave select signals)
- Programmable clock phase and polarity
- Optional transmit and receive FIFOs
- Local loopback capability for testing

## Ethernet 10/100 MAC

- 32-bit OPB master and slave interfaces
- Media Independent Interface (MII) for connection to external 10/100 Mbps PHY Transceivers
- Full and half duplex modes of operation
- Supports unicast, multicast, broadcast, and promiscuous addressing
- Provides auto or manual source address, pad, and Frame Check Sequence

## Ethernet 10/100 MAC (cont)

- Simple DMA and Scatter/Gather DMA architecture for low processor and bus utilization, as well as a simple memory-mapped direct I/O interface
- Independent 2K to 32K transmit and receive FIFOs
- Supports MII management control writes and reads with MII PHYs
- Supports VLAN and Pause frames
- Internal loopback mode

## 1 Gigabit MAC

- 64-bit PLB master and slave interfaces
- GMII for connection to external PHY Transceivers
- Optional PCS function with Ten Bit Interface (TBI) to external PHY devices
- Option PCS/PMA functions with SerDes interface to external transceiver devices for reduced signal count
- Full duplex only
- Provides auto or manual source address, pad, and Frame Check Sequence

## 1 Gigabit MAC (cont)

- Simple DMA and Scatter/Gather DMA architecture for low processor and bus utilization, as well as a simple memory-mapped direct I/O interface
- Independent, depth-configurable TX and RX FIFOs
- Supports MII management control writes and reads with MII PHYs
- Jumbo frame and VLAN frame support
- Internal loopback mode

## Single Channel HDLC

- Support for a single full duplex HDLC channel
- Selectable 8/16 bit address receive address detection, receive frame address discard, and broadcast address detection
- Selectable 16 bit (CRC-CCITT) or 32 bit (CRC-32) frame check sequence
- Flag sharing between back to back frames
- Data rates up to OPB_Clk frequency

## Single Channel HDLC (cont)

- Simple DMA and Scatter/Gather DMA architecture for low processor and bus utilization, as well as a simple memory-mapped direct I/O interface
- Independent, depth-configurable TX and RX FIFOs
- Selectable broadcast address detection and receive frame address discard
- Independent RX and TX data rates

## ATM Utopia Level 2

- UTOPIA Level 2 master or slave interface
- UTOPIA interface data path of 8 or 16 bits
- Single channel VPI/VCI service and checking in received cells
- Header error check (HEC) generation and checking
- Parity generation and checking
- Selectively prepend headers to transmit cells, pass entire received cells or payloads only, and transfer 48 byte ATM payloads only

## ATM Utopia Level 2 (cont)

- Simple DMA and Scatter/Gather DMA architecture for low processor and bus utilization, as well as a simple memory-mapped direct I/O interface
- Independent, depth-configurable TX and RX FIFOs
- Interface throughput up to 622 Mbps (OC12)
- Internal loopback mode

## OPB-PCI Bridge

- 33/66 MHz, 32-bit PCI buses
- Full bridge functionality
  - OPB Master read/write of a remote PCI target (both single and burst)
  - PCI Initiator read/write of a remote OPB slave (both single and multiple)
- Supports up to 3 PCI devices with unique memory PCI memory space
- Supports up to 6 OPB devices with unique memory OPB memory space
- PCI and OPB clocks can be totally independent

## System ACE Controller

- Used in conjunction with System ACE CompactFlash Solution to provide a System ACE memory solution.
- System ACE Microprocessor Interface (MPU)
  - Read/Write from or to a CompactFlash device
  - MPU provides a clock for proper synchronization
- ACE Flash (Xilinx-supplied Flash Cards)
  - Densities of 128 MBits and 256 Mbits
  - CompactFlash Type 1 form factor
    - Supports any standard CompactFlash module, or IBM microdrives up to 8 Gbits, all with the same form factor.
- Handles byte, half-word, and word transfers

## GPIO

- OPB V2.0 bus interface with byte-enable support
- Supports 32-bit bus interface
- Each GPIO bit dynamically programmable as input or output
- Number of GPIO bits configurable up to size of data bus interface
- Can be configured as inputs-only to reduce resource utilization

## Memory Controllers

- PLB and OPB interfaces
- External Memory Controller
  - Synchronous Memory (ZBT)
  - Asynchronous Memory (SRAM, Flash)
- Internal Block Memory (BRAM) Controllers
- DDR and SDRAM

## Creating a Simple MicroBlaze System with EDK

## Design Flow

- Design Entry with Xilinx Platform Studio
- Generate system netlist with XPS
- Generate hardware bitstream with XPS
- Download and sanity check design with XPS and XMD

## Simple MicroBlaze System Block Diagram