Logic analyzers and testing

- Logic analyzers
- Testing: The big picture
- Debugging

3 tools for testing

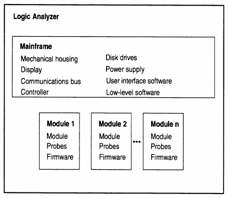
- 1. The oscilloscope
  - Shows electrical details
    - Benefits: Wideband, accurate
    - Disadvantages: < 4 inputs; triggering
- 2. The logic analyzer
  - Shows thresholded data
    - Benefits: Many channels, trigger on patterns
    - Disadvantages: Idealized waveforms, insufficient access
- 3. Embedded test
  - *You* design in built-in test features
    - Benefits: Only way to test large chips
    - Disadvantages: Uses chip area, incomplete scan, difficult design

Logic analyzers

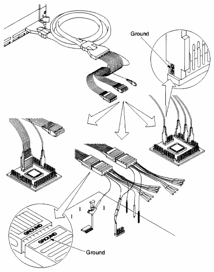
- Instruments for acquiring digital data
  - Wide data "bus"
  - Memory stores bus data
  - Smart triggering decides what data to store
  - Embedded computer processes the data
- We use the Tektronix TLA714-716
  - 132 channels
  - 32k memory per channel
  - 100MHz state
  - 2GSPS sampling
  - Win2k interface

Logic analyzer physical model

- A mainframe
  - Housing, bus, controller, UI
- Plug-in modules
  - Modules acquire data
  - Ours TLAs have 4 7L1 modules
    - 32k memory depth
    - 100MHz state
    - 32 data and 2 clock each
- Probe pods
  - Pods are wire bundles
  - Probes attach to your circuit
    - We have P6417 probes

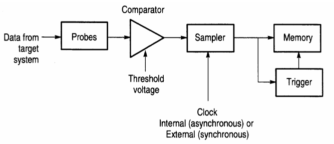


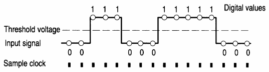
Probe pods



Logic analyzer conceptual model

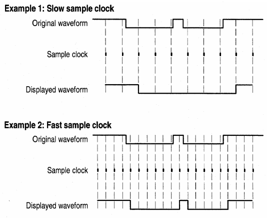
- All parameters are adjustable
  - Threshold voltage
  - Clock rate
  - Trigger conditions
  - Memory depth





Clocking a logic analyzer

- Samples data every clock cycle
- External/synchronous clocking
  - You supply the clock
  - Use when you need to see long data records
    - Analyzer stores one sample per clock period
- Internal/asynchronous clocking
  - Analyzer supplies the clock
    - 4ns to 50ms
  - Use when you need to see precise timing
    - Find glitches


Example 1: Slow sample clock

Example 2: Fast sample clock

Triggering and acquisition

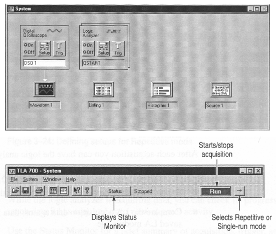
- Derive trigger from sampled data
  - Data values
  - Data ranges
  - Signals from another module
  - Internal counters
- Data acquisition in continuous
  - Memory is a circular buffer
  - New samples continually overwrite oldest samples
  - Trigger tells the acquisition to stop
- Triggers can qualify acquisition
  - Store only selected data

Modules are semi-autonomous

- Each module has its own setup
  - Its own clock
  - Its own trigger
  - Acquires and stores its own data
- Modules communicate via their trigger programs
  - Can trigger all modules
  - Or have one module arm another
- All data is time correlated
  - Regardless of the module

System window

- Top-level in hierarchy
  - Open other windows
    - Module
    - Data
  - Create new data, listing, and waveform windows
  - Shows which modules are associated with a data window
  - Enable/disable modules
  - Save and load files



Starts/stops acquisition

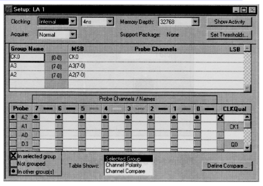
Displays Status Monitor

Selects Repetitive or Single-run mode

- *Note: We don't have DSO modules

Module setup window

- Each module has its own setup and trigger windows
  - Set up each module independently
- Set all parameters
  - Assign channels to groups
  - Thresholds
  - Clock rate
  - Comparisons
- Configure setup before trigger
  - Trigger settings depend on the module settings


Setup: LA 1

Clocking: Internal 4ns

Memory Depth: 32768

Acquire: Normal

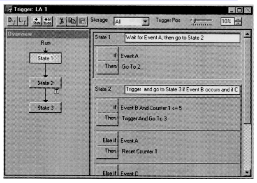
Support Package: None

Group Name		MSB Probe Channels LSB
CK0	(0-0)	CK0
A3	(7-0)	A3(7-0)
A2	(7-0)	A2(7-0)

Table Shows: Selected Group

Module trigger window

- Triggering is the ***key*** feature of a logic analyzer
  - Tells the analyzer how to find the data that you want
    - Trigger off a data pattern
    - Trigger off a data sequence
  - Multiple states
    - Multiple clauses per state
- Analyzer has a trigger library!
- Logic analyzers are designed for non-repetitive data
  - Unlike an oscilloscope


Trigger: LA 1

Storage: All

Trigger Pos 10%

State 1 Wait for Event A, then go to State 2

If Event A

Then Go To 2

State 2 Trigger and go to State 3 if Event B occurs and if C

If Event B And Counter 1 <= 5

Then Trigger And Go To 3

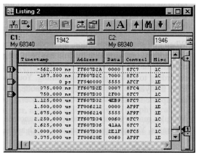
Else If Event A

Then Reset Counter 1

Else If Event C

Data windows

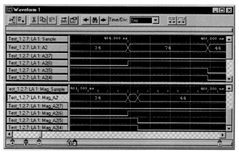
- Many types
  - Listing window
  - Waveform window
  - Histogram window
  - Source-data window
- Features common to all
  - Cursors
  - Flags
  - Scroll
  - Search



Listing 2

C1: My 68340 1942 C2: My 68340 1946

```
Timestamp           Address    Data  Control  Misc
   -562.500 ns      FF607D2A   0000  8FC7     1C
   -187.500 ns      FF607D2C   7000  8FC5     1C
          0 ps      FF540000   5555  AFCF     1E
    375.000 ns      FF607D2E   3007  8FC4     1C
    750.000 ns      FF607D30   2F00  8FC7     1C
  1.125,000 us      FF607D32   4EB9  8FC7     1C
  1.500,000 us      FF006212   0000  AF9F     1E
  1.875,000 us      FF006214   5555  AF9F     1E
  2.250,000 us      FF607D34   0060  8FC7     1C
  2.625,000 us      FF607D36   41AA  8FC7     1C
  3.000,000 us      FF607D38   2E1F  8FC5     1C
  3.375,000 us      FF00620E   0060  AF9F     1E
```

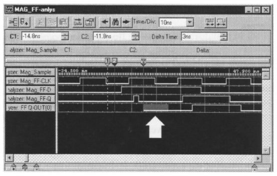


Waveform 1

Time/Div: 1ns

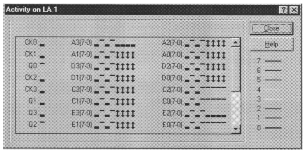
Capturing glitches

- Trigger on the glitch
  - Triggering looks for multiple transitions in a clock cycle
  - Captures dynamic hazards
- Can also trigger on setup and hold violations



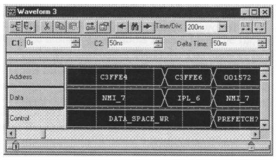
Other features: Activity indicator

- How do you know if a pod is active?
  - Hooked up properly?
  - Seeing data?



Other features: Programmability

- Symbols
  - You define in a LUT
  - Analyzer assigns symbols to data patterns
- User programs
  - e.g. export to file and continue



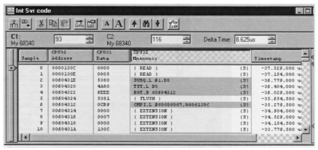
Waveform 3

Time/Div: 200ns

C1: 0s C2: 50ns Delta Time: 50ns

Other features: µP support

- Analyzer disassembles data to µP mnemonics
- Requires special module podsets



Int Svr code

C1: My 68340 93 C2: My 68340 116 Delta Time: 8.625us

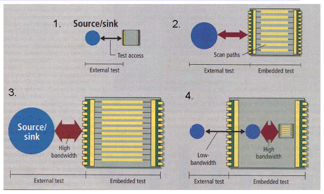
```
Sample  CPU32     CPU32  CPU32                                 Timestamp
        Address   Data   Mnemonic
     0  0000130C  0000   ( READ )                       (S)   -37.529,000 us
     1  0000130E  0005   ( READ )                       (S)   -37.154,000 us
     2  0060431E  5380   SUBQ.L #1,D0                   (S)   -36.779,000 us
     3  00604320  4A80   TST.L D0                       (S)   -36.404,000 us
     4  00604322  6EEE   BGT.B 00604312                 (S)   -36.029,000 us
     5  00604324  5381   ( FLUSH )                      (S)   -35.654,500 us
     6  00604312  0CB9   CMPI.L #00000007,0000130C      (S)   -35.279,500 us
     7  00604314  0000   ( EXTENSION )                  (S)   -34.904,000 us
     8  00604316  0007   ( EXTENSION )                  (S)   -34.529,000 us
     9  00604318  0000   ( EXTENSION )                  (S)   -34.154,500 us
    10  0060431A  130C   ( EXTENSION )                  (S)   -33.779,500 us
```

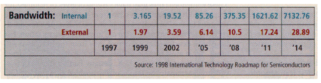
Testing: The big picture

- The difference between internal and external BW has driven test technology
  1. External test
  2. Embedded scan path
  3. High-BW embedded
  4. Embedded source
  5. ???

External BW ≡ (# of I/O) * (external clock rate)

Internal BW ≡ (# of transistors)* (internal clock rate)





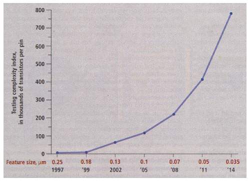
Bandwidth:							
Internal	1	3.165	19.52	85.26	375.35	1621.62	7132.76
External	1	1.97	3.59	6.14	10.5	17.24	28.89
	1997	1999	2002	'05	'08	'11	'14

Source: 1998 International Technology Roadmap for Semiconductors

From IEEE Spectrum, 7/99, pgs. 55 / 57

Semiconductor scaling confounds testing

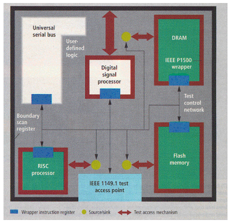
- Testing is a key obstacle to future advancement in digital technology
- Need to ensure logic functionality
  - Despite ever-more-limited access to internal logic
- Testing at the board, subsystem, and system level becomes ever harder



From IEEE Spectrum, 7/99, p. 55

System-on-a-chip testing

- IEEE P1500 standard
  - For embedded core test
  - In development
- Standardized core test language
- Standardized core test wrapper
  - Configurable
  - Scalable



From IEEE Spectrum, 7/99, p. 59

Debugging

- It doesn't work, now what?