Electrical realities

- Today
  - Review basic electronics
  - Some real-world examples
  - Fixed-function logic
  - Oscilloscopes

Basic electronics

- What you should know
  - Voltage and current
  - Resistors
  - Capacitors
  - Inductors
  - Time constants
  - Bandwidth and risetime

Current and voltage

- Current is the flow of charge
  - Assume positively charged particles
    - Real physical current is negatively charged electrons
  - Units are amps; we will use mA (10^{-3}A) or μA (10^{-6}A)
    - 1 amp = 1 coulomb/sec
  - 1 electron has a charge of -1.6×10^{-19} coulombs
- Voltage is a measure of potential energy
  - Work that can be done by the electrons
  - Must *always* have a reference; we will use ground
  - Units are volts; we will use V or mV (10^{-3}V)

Energy and power

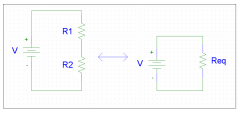
- Energy is measured in joules
  - Raising the potential of 1 coulomb of (positive) charge by 1V takes 1 joule of energy
- Power is measured in Watts
  - Energy per unit time
    - Joules/second
  - In a circuit, P = IV
    - in Watts = Joules/second

Resistors

- Ohm's law: $v = iR$
- $\text{Energy} = \int_0^t ivdt = \int_0^t i^2 R dt = I^2 R t$ (assuming $i = \text{constant} \equiv I$)
  - $i \equiv$ current (time varying); $I \equiv$ current (d.c.)
  - $v \equiv$ voltage; $R \equiv$ resistance
- $\text{Power} = \frac{dE}{dt} = I^2 R$

Resistors (con't)

Resistors in series

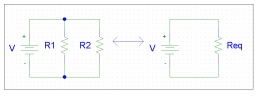


$$V - iR_1 - iR_2 = 0$$

$$i = \frac{V}{R_1 + R_2} = \frac{V}{R_{eq}}$$

$$R_{eq} = R_1 + R_2$$

Resistors in parallel

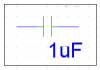


$$i_1 = \frac{V}{R_1} \qquad i_2 = \frac{V}{R_2} \qquad i_{total} = i_1 + i_2$$

$$\frac{V}{R_{eq}} = i_{total} = \frac{V}{R_1} + \frac{V}{R_2}$$

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2}$$

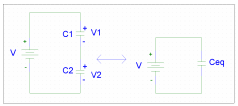
Capacitors



- $q = CV \qquad i = \frac{dq}{dt} = C\frac{dV}{dt}$
- Energy $= \int_0^\infty ivdt = \int_0^\infty CV\frac{dV}{dt}dt = C\int_0^{V_C(t=\infty)} VdV = \frac{1}{2}CV^2$
  - $q \equiv$ charge; $i \equiv$ current $= dq/dt$
  - $v \equiv$ voltage; C $\equiv$ capacitance
- Power $= \frac{dE}{dt} = 0$
  - Capacitors are dissipationless

Capacitors (con't)

Capacitors in series

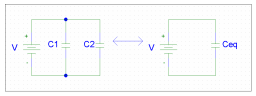


$V_1 = \frac{q}{C_1} \qquad V_2 = \frac{q}{C_2} \qquad V = V_1 + V_2$

$\frac{q}{C_{eq}} = V = \frac{q}{C_1} + \frac{q}{C_2}$

$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}$

Capacitors in parallel



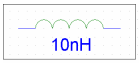
$q_1 = C_1V \qquad q_2 = C_2V \qquad q_{eq} = C_{eq}V$

$q_{eq} = q_1 + q_2$

$C_{eq}V = C_1V + C_2V$

$C_{eq} = C_1 + C_2$

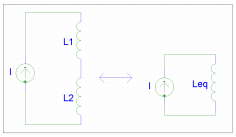
Inductors



- $\Phi = Li \qquad V = \frac{d\Phi}{dt} = L\frac{di}{dt}$
- Energy $= \int_0^\infty ivdt = \int_0^\infty Li\frac{di}{dt}dt = L\int_0^{I_L(t=\infty)} idi = \frac{1}{2}LI^2$
  - $\Phi \equiv$ flux; $v \equiv$ voltage $= d\Phi/dt$
  - $i \equiv$ current; L $\equiv$ inductance
- Power $= \frac{dE}{dt} = 0$
  - Inductors are dissipationless

Inductors (con't)

Inductors in series



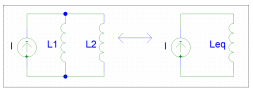
$\Phi_1 = L_1I \qquad \Phi_2 = L_2I \qquad \Phi_{eq} = L_{eq}I$

$\Phi_{eq} = \Phi_1 + \Phi_2$

$L_{eq}I = L_1I + L_2I$

$L_{eq} = L_1 + L_2$

Inductors in parallel

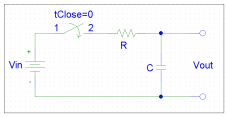


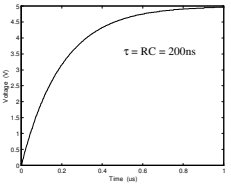
$I_1 = \frac{\Phi}{L_1} \qquad I_2 = \frac{\Phi}{L_2} \qquad I = I_1 + I_2$

$\frac{\Phi}{L_{eq}} = I = \frac{\Phi}{L_1} + \frac{\Phi}{L_2}$

$\frac{1}{L_{eq}} = \frac{1}{L_1} + \frac{1}{L_2}$

Time constants





$V_{in} = v_r + V_{out} \qquad v_r = iR \qquad i = C\frac{dV_{out}}{dt}$

$V_{in} = iR + V_{out}$

$V_{in} = RC\frac{dV_{out}}{dt} + V_{out}$

$-RCdV_{out} = (V_{out} - V_{in})dt$

$-\frac{dt}{RC} = \frac{dV_{out}}{(V_{out} - V_{in})}$

$-\frac{1}{RC}\int_0^t dt = \int_0^{V_{out}(t)} \frac{dV_{out}}{(V_{out} - V_{in})}$

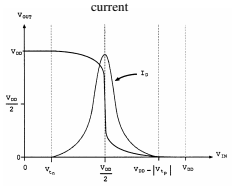
$-\frac{t}{RC} = \ln(V_{out}(t) - V_{in}) - \ln(-V_{in})$

$V_{out}(t) = V_{in}\left(1 - e^{-\frac{t}{RC}}\right)$

Transient power

- Synchronous (clocked) circuits have huge transient supply currents
  - Logic elements switch simultaneously
  - Peak current is orders of magnitude larger than static current
- Wire resistance and inductance causes transient voltage bounce on power bus

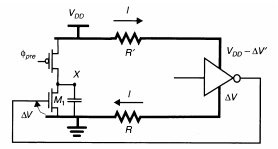
CMOS inverter switching threshold and short-circuit current



Power and ground bounce

- Bus drops reduce logic-gate voltages
  - Switching currents are smaller
  - Logic gates are slower
- Bus drops reduce noise margins
  - Especially for low-voltage logic
  - Can cause bit errors!

- Inverter has less output current
- Bus drop can cause M_1 to erroneously discharge node *X*

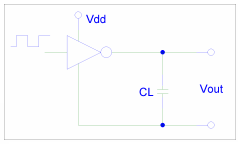


Example 1

- You must test a high-speed FPGA
  - Output rise times (10% – 90%) are 2ns
- What is the minimum scope bandwidth?
  - For you to see rising edges reliably

Example 2

- An inverter drives a 50pF load capacitor at 100MHz
  - How much power does it dissipate driving the load?



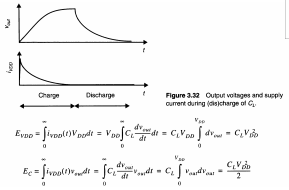


Figure 3.32 Output voltages and supply current during (dis)charge of C_L

$$E_{VDD} = \int_0^\infty i_{VDD}(t) V_{DD} dt = V_{DD} \int_0^\infty C_L \frac{dv_{out}}{dt} dt = C_L V_{DD} \int_0^{V_{DD}} dv_{out} = C_L V_{DD}^2$$

$$E_C = \int_0^\infty i_{VDD}(t) v_{out} dt = \int_0^\infty C_L \frac{dv_{out}}{dt} v_{out} dt = C_L \int_0^{V_{DD}} v_{out} dv_{out} = \frac{C_L V_{DD}^2}{2}$$

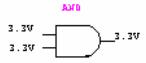
$$\text{Power} = C_L V_{dd}^2 f$$
$$= (50\times10^{-12}\,\text{F})(5\text{V})^2(100\times10^6)$$
$$= 125\text{mW}$$

Example 3

- A processor IC has a transient (surge) current of 12A every time the clock switches. The surge risetime is 2ns.
  - The PCB trace resistance is 0.15Ω
    - What is the resistive voltage drop
    - $V_R = iR = (12\text{A})(0.15\Omega) = 180\text{mV}$
  - The chip uses 20 V_{dd} bondwires, each with an inductance of 1nH
    - What is the inductive voltage drop
    - $V_L = L\frac{di}{dt} = \left(\frac{1\text{nH}}{20}\right)\left(\frac{12\text{A}}{2\text{ns}}\right) = 300\text{mV}$

IC Logic levels, voltage, & definitions

- Logic gates operate on real physical voltages



"1" == high voltage
"0" == low voltage

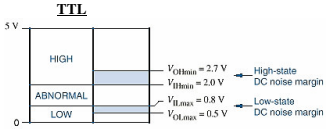
AND Gate
"1" AND "1" = "1"

- We cannot guarantee precise voltages, so we allow a range
  - V_{oh} ≡ minimum output voltage high
  - V_{ol} ≡ maximum output voltage low
  - Guaranteed logic swing ≡ $V_{oh} - V_{ol}$
  - V_{ih} ≡ minimum input voltage high
  - V_{il} ≡ maximum input voltage low
  - Noise margin: $NM_L = V_{il} - V_{ol}$ $NM_H = V_{oh} - V_{ih}$

TTL and CMOS logic levels

- TTL ≡ Transistor-transistor logic (bipolar transistors)
- CMOS ≡ Complementary metal oxide semiconductor
- TTL I/O are closer to ground than CMOS
  - Logic families not 100% compatible
  - More about this later

TTL



CMOS

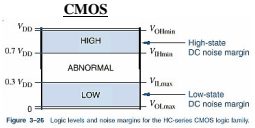
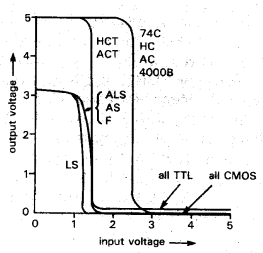


Figure 3–26 Logic levels and noise margins for the HC-series CMOS logic family.

TTL/CMOS Transfer Characteristics



More definitions

- Propagation delay: The delay through a gate
  - Measured at the 50% points on the input and output waveforms
  - Has a range: min/typical/max
  - Depends on the fanout
    - The number of loads the gate drives
  - Your design must work over the entire delay range
- Rise and fall times: Time for a signal to transition
  - Typically measured at 10% to 90% of the logic swing
    - Sometimes at 20% to 80%
- Pulse width — time that an output stays high
  - Duty cycle ≡ (pulse width) ÷ (pulse period)
  - Frequency ≡ 1 / period

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC54/74HC374

Octal 3-State Noninverting D Flip-Flop
High-Performance Silicon-Gate CMOS

The MC54/74HC374 is identical in pinout to the LS374. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state; thus, data may be stored even when the outputs are not enabled.

The MC574 is identical in function to the HC574, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HC534, which has inverting outputs.

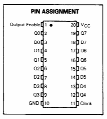
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 286 FETs or 65.5 Equivalent Gates

J SUFFIX CERAMIC CASE 732-03
N SUFFIX PLASTIC CASE 738-03
DW SUFFIX SOIC CASE 751D-03

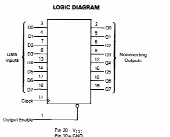
ORDERING INFORMATION
MC74HC374N Plastic
MC54HC374J Ceramic
MC74HC374DW SOIC

T_A = –55° to 125°C for all packages.
Dimensions in Chapter 6

PIN ASSIGNMENT



LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Output
Output Enable	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	–65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit –55°C to 25°C	≤85°C	≤125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V; $\|I_{out}\| \le 20$ µA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V; $\|I_{out}\| \le 20$ µA	2.0	0.5	0.5	0.5	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL}; $\|I_{out}\| \le 20$ µA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in} = V_{IH} or V_{IL}; $\|I_{out}\| \le 6.0$ mA	4.5	3.98	3.84	3.70	
		$\|I_{out}\| \le 7.8$ mA	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL}; $\|I_{out}\| \le 20$ µA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in} = V_{IH} or V_{IL}; $\|I_{out}\| \le 6.0$ mA	4.5	0.26	0.33	0.40	
		$\|I_{out}\| \le 7.8$ mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	µA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State; V_{in} = V_{IL} or V_{IH}; V_{out} = V_{CC} or GND	6.0	±0.5	±5.0	±10.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND; I_{out} = 0 µA	6.0	8	80	160	µA

NOTE: Information on typical parametric values can be found in Chapter 4.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit 25°C to –55°C	≤85°C	≤125°C	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	180	225	270	ns
		4.5	36	45	54	
		6.0	31	38	46	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V	40	pF

TIMING REQUIREMENTS (Input t_r = t_f = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit 25°C to –55°C	≤85°C	≤125°C	Unit
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t_h	Minimum Hold Time, Clock to Data (Figure 3)	2.0	25	30	40	ns
		4.5	5	6	8	
		6.0	5	6	7	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

SWITCHING WAVEFORMS

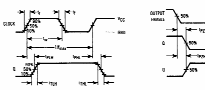


Figure 1.

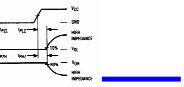


Figure 2.

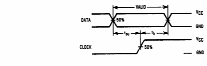
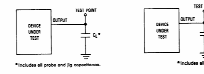


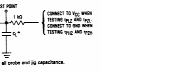
Figure 3.

TEST CIRCUITS



*Includes all probe and jig capacitance.

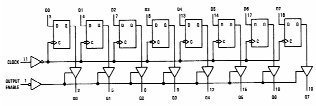
Figure 4.



*Includes all probe and jig capacitance.

Figure 5.

EXPANDED LOGIC DIAGRAM



Comparing logic families

Table 1. Logic Family Comparisons

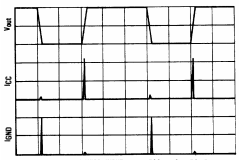
General Characteristics (1) (All Maximum Ratings)

Characteristic	Symbol	TTL		CMOS		Unit
		LS	ALS	MC14000	HI-Speed	
Operating Voltage Range	$V_{CC/EE/DD}$	5±5%	5±5%	3.0 to 18	2.0 to 6.0	V
Operating Temperature Range	T_A	0 to +70	0 to +70	−40 to +85	−55 to +125	°C
Input Voltage (limits)	V_{IH} min	2.0	2.0	3.5[4]	3.5[4]	V
	V_{IL} max	0.8	0.8	1.5[4]	1.0[4]	V
Output Voltage (limits)	V_{OH} min	2.7	2.7	V_{DD}−0.05	V_{CC}−0.1	V
	V_{OL} max	0.5	0.5	0.05	0.1	V
Input Current	I_{INH}	20	20	±0.3	±1.0	μA
	I_{INL}	−400	−200			
Output Current @ V_O (limit) unless otherwise specified	I_{OH}	−0.4	−0.4	−2.1 @ 2.5 V	−4.0 @ V_{CC}−0.8 V	mA
	I_{OL}	8.0	8.0	0.44 @ 0.4 V	4.0 @ 0.4 V	mA
DC Noise Margin Low/High	DCM	0.3/0.7	0.3/0.7	1.45[4]	0.90/1.35[4]	V
DC Fanout	–	20	20	>50(1)[2]	50(10)[2]	–

Electrical realities

- ICs draw lots of current when switching
  - Power supply is typically far away
    - Many nanoseconds of wire
  - The chip supply voltage will drop
    - Degrading the outputs
- Add decoupling
  - A capacitor from V_{dd} to Gnd
    - Right at the chip pins
  - Keeps voltage from dropping
    - $I = C dV/dt$
- Tie unused chip inputs to gnd
  - Prevents random switching

From Motorola HC data book



BUFFERED DEVICE: INPUT $t_r, t_f \le 500$ ns, $C_L = 50$ pF

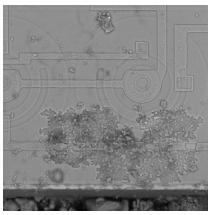
Figure 46. Switching Currents for $C_L = 50$ pF

Electrostatic discharge (ESD)

- Triboelectric charging: Charge transfer due to the contact and separation of materials
  - Electrons transfer from one material to the other
  - ***You*** can acquire 5 – 15 thousands of volts of static charge
    - By walking on carpet or moving your clothes or...
- ESD: Charge transfer between bodies at different potentials
  - You feel a shock when you touch something
  - This shock will kill a chip
- Most ICs have input protection
  - But only good to about 2000V

ESD damage

- Due to poor handling practices
  - Usually people not discharging themselves before touching chips
- Failure types
  - Catastrophic
    - Chip dies immediately
  - Latent defects
    - Chip dies early in life



SEM photo of chip failure due to electrical overstress
http://www.sem-lab.com/

Eliminating ESD

- Design for ESD
  - Use protection circuitry
  - Use proper packaging
- Reduce charge generation
  - Wear cotton clothing
  - Keep humidity up
  - Use conductive packaging
- Dissipate charge
  - Use ground straps, ground mats, etc.
  - Ground yourself before touching an IC

Oscilloscopes

- Measure voltage as a function of time
  - Vertical scale is in volts/division
    - Set using scale knob
  - Horizontal scale is time/division
    - Set using timebase
- You tell the scope when to acquire data
  - You trigger the scope
    - Tell it to capture a 10,000 point waveform (Normal mode)
  - The trigger can be any event
    - Another signal
    - Some feature of your signal
  - The trigger must be correlated with your waveform
    - Else successive acquisitions will look random

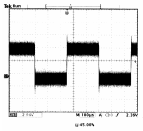
Triggering oscilloscopes (con't)

- Normal trigger mode
  - Scope triggers continuously
- Pretriggering and delay
  - You tell the scope when to take data relative to the trigger
- Single-shot acquisition
  - You tell the scope to trigger once and stop
- Trigger icons help you
  - Trigger-position icon: Shows the trigger location in the waveform
  - Trigger-level icon: Shows the trigger voltage level on the waveform
  - Waveform-record icon: Shows the trigger location in the record

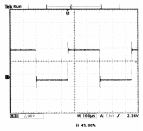
Oscilloscope features

- Measurement
  - Cursors measure voltage, time, frequency
  - Autoset configures the scope for you
- Signal processing
  - Averaging multiple waveforms reduces noise
  - Envelope captures maximum variation of a signal
  - Can do math on waveforms

noisy trace



with averaging



Oscilloscope probing

- Probes have 2 terminals
  - Center conductor: Signal
  - Outer conductor: Ground
- You must supply a good ground
  - Voltage reference for the scope
  - Return path for current that goes up the probe
    - Recall Kirchoff's laws
- Our scopes have 2 or 4 channels
  - Can probe 2 or 4 signals simultaneously
  - They must be related in frequency