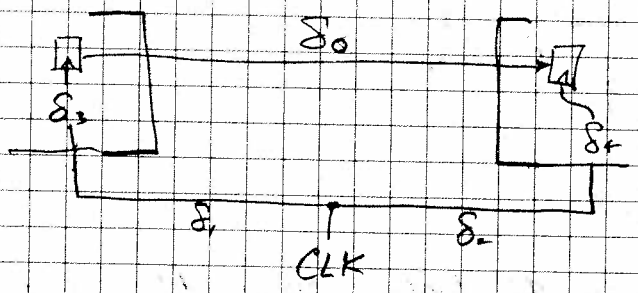
Source Synchronous

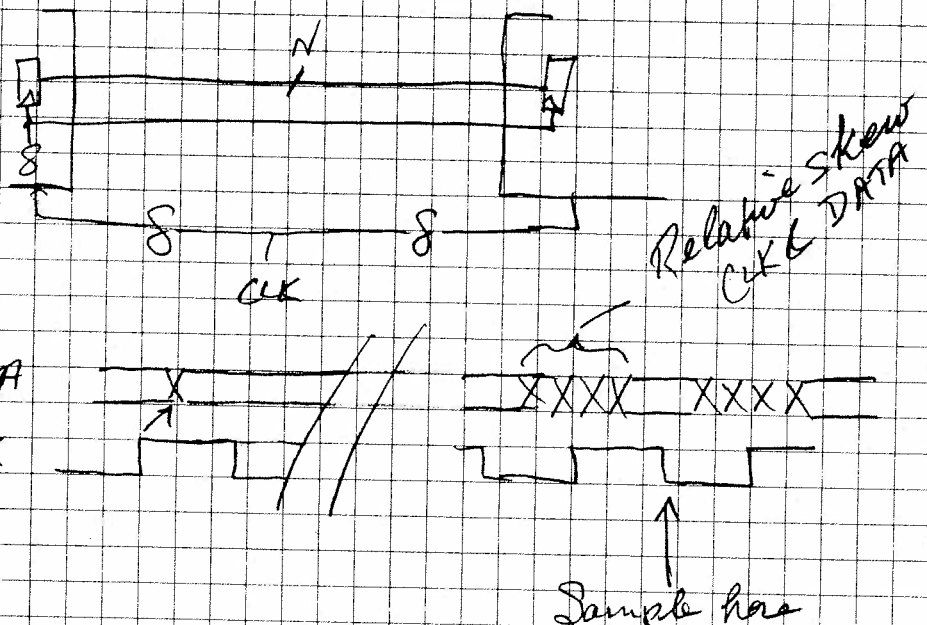


Clock skew may be significant

δ_0 may be large

$\Rightarrow$ Very slow clock.

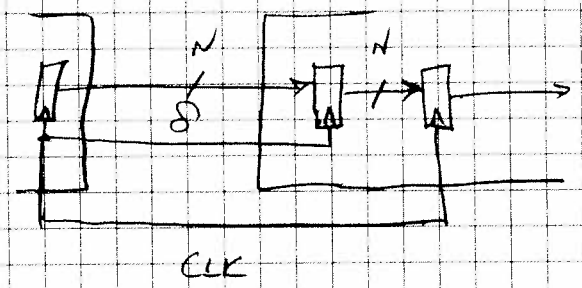
IDEA: Match delays: Send clock with Data!



Note: δ_0 can be larger than clock period!

We still have a problem...

Source Synchronous (2)



We now have arbitrary skew between the source clock and system clock.

Solution?

1. Agnostic: Use async. FIFO (problem?)
2. Compute phase difference

Fixed?