Signal Integrity

Friday June 25 2011

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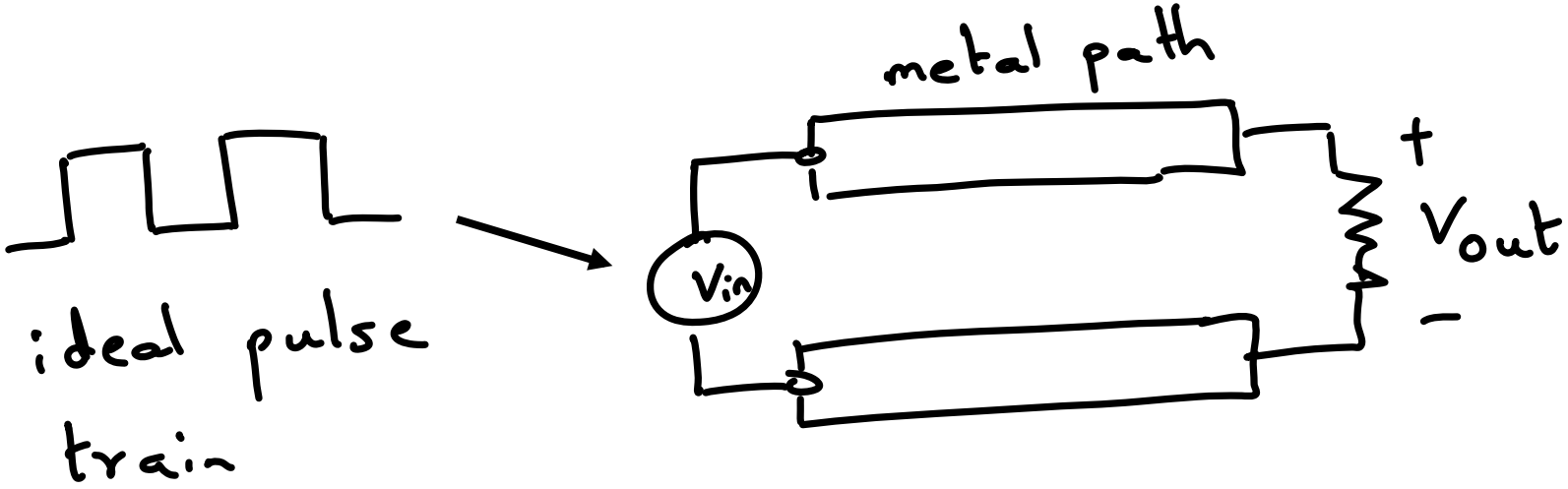
What is signal integrity ?

- The challenges and problems that arise in high-speed products due to propagation path effects

- Especially in interconnects
  - On-chip
  - Chip-to-Chip
  - Package
  - Board
  - Backplane

Transmission Line Example



- What do you expect to see at V_{out} ?

Delay

- "Time of Flight": Related to velocity of light and distance.

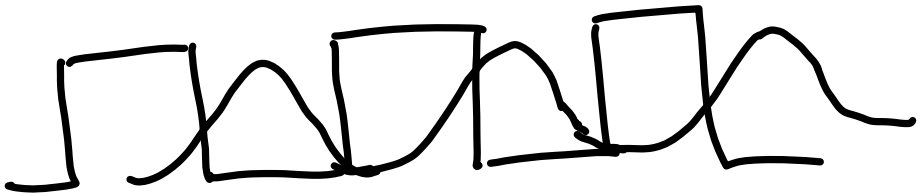
Example: 1 mm trace :, vel. of light in medium $\approx \frac{1}{} \times 10^{8}$ m/s

Delay : $\frac{10^{-3}}{10^{8}} : 10^{-11}$ s : 10 ps

10 cm server backplane global trace : $\frac{10^{-1}}{10^{8}} : \frac{1}{}$ ns

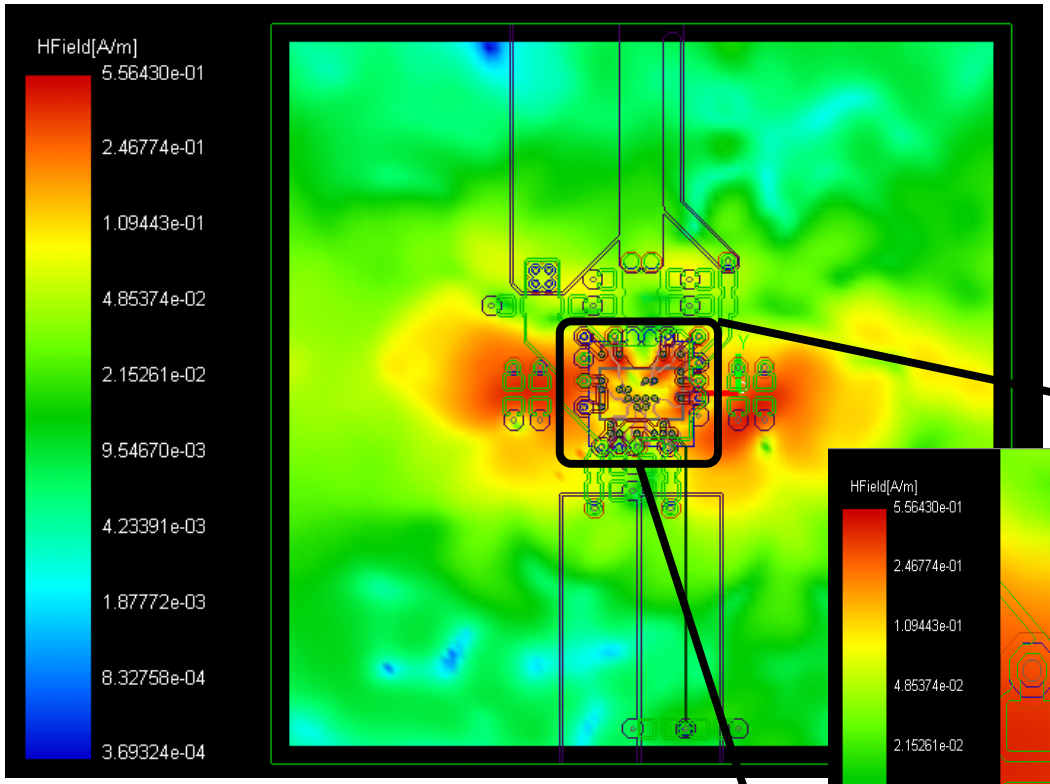
Loss

- (Typically) Higher frequency components are “attenuated”



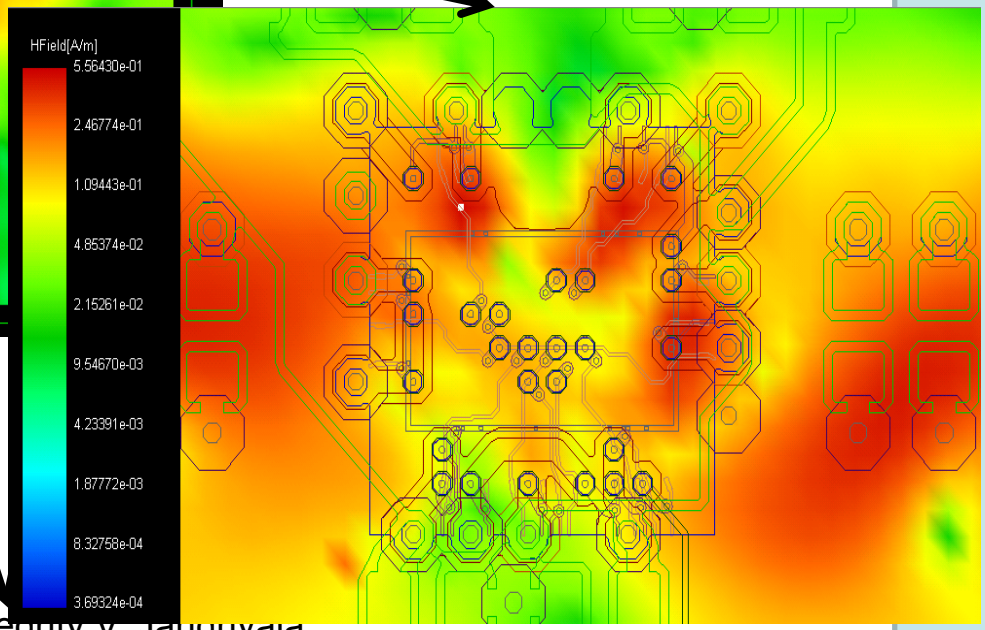
- Loss caused by
  - Metal
  - Material (Dielectric)
  - Radiation

EMI Radiation



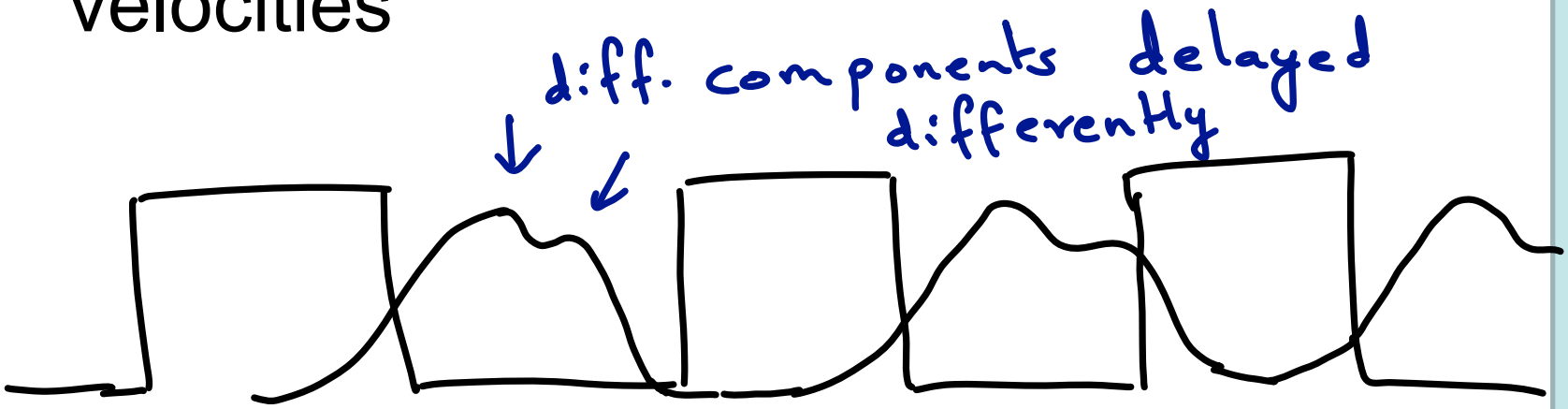
Courtesy: Physware

Transistor switching on chip causing system-level radiation hotspots



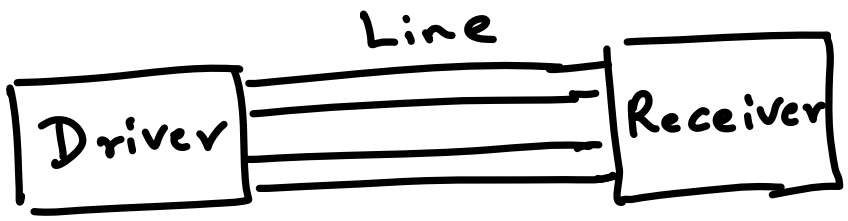
Dispersion

- Different frequencies travel at different velocities



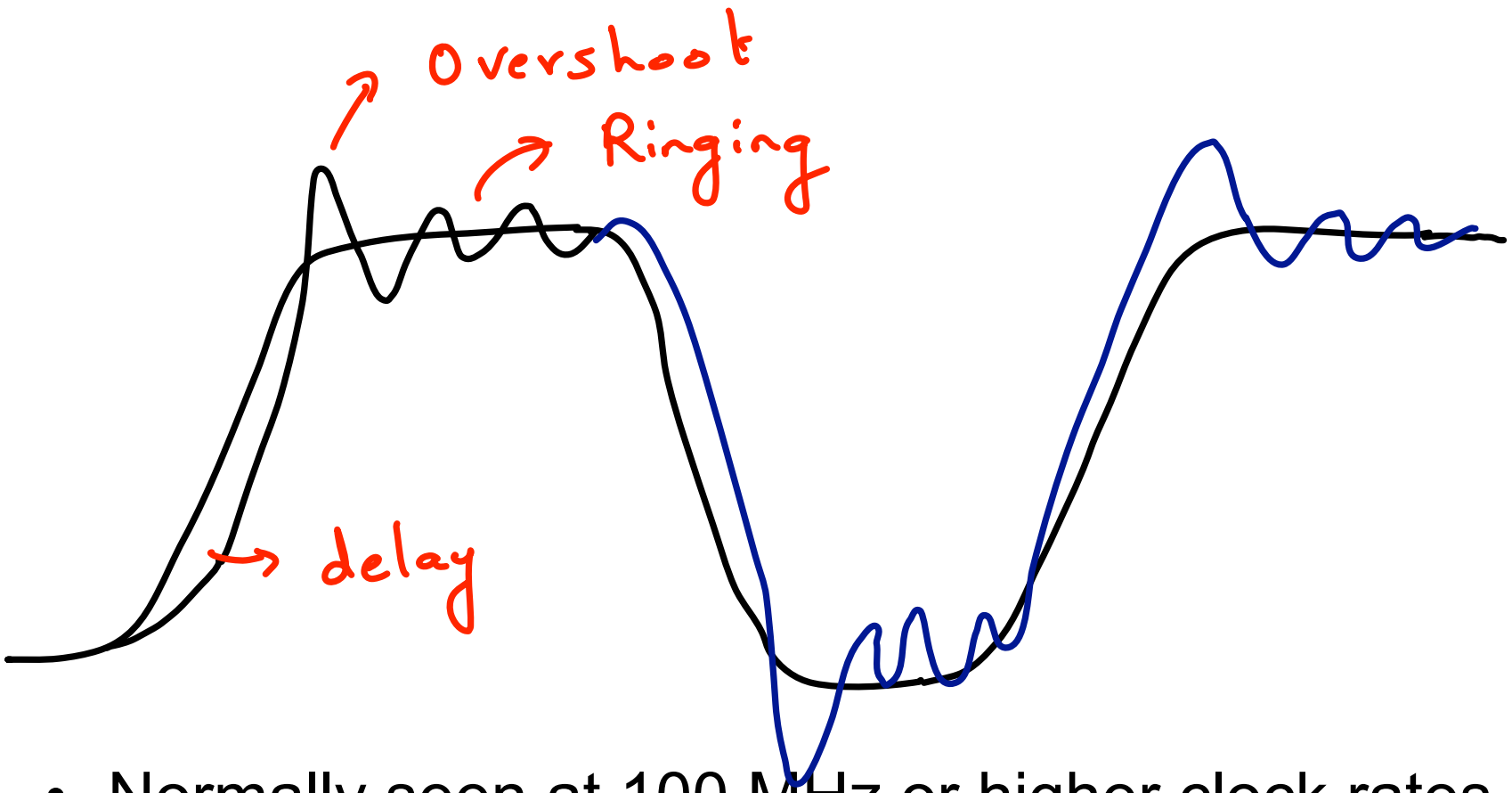
Mismatch

- Driver impedance
- Line impedance
- Receiver impedance (input)



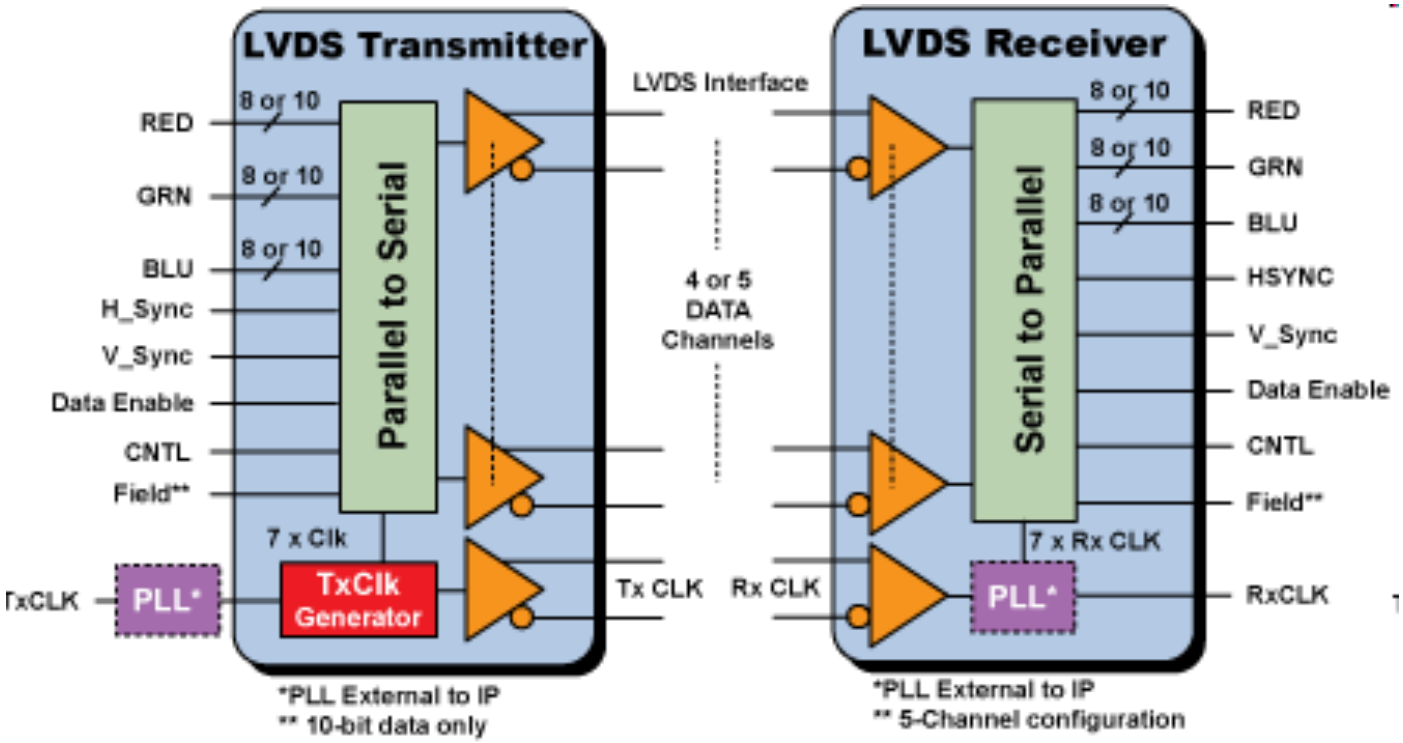
- Any mismatch causes additional effects

Mismatch

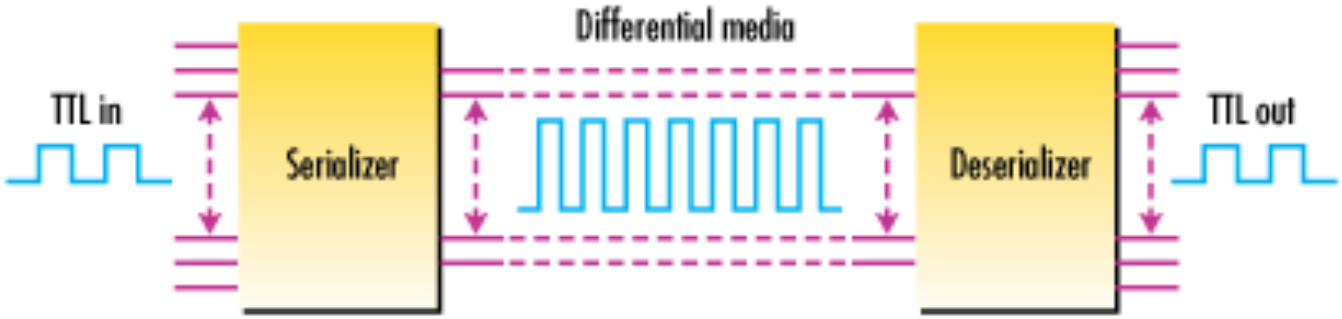


- Normally seen at 100 MHz or higher clock rates

Serialization-Deserialization



Serdes:Differential signaling



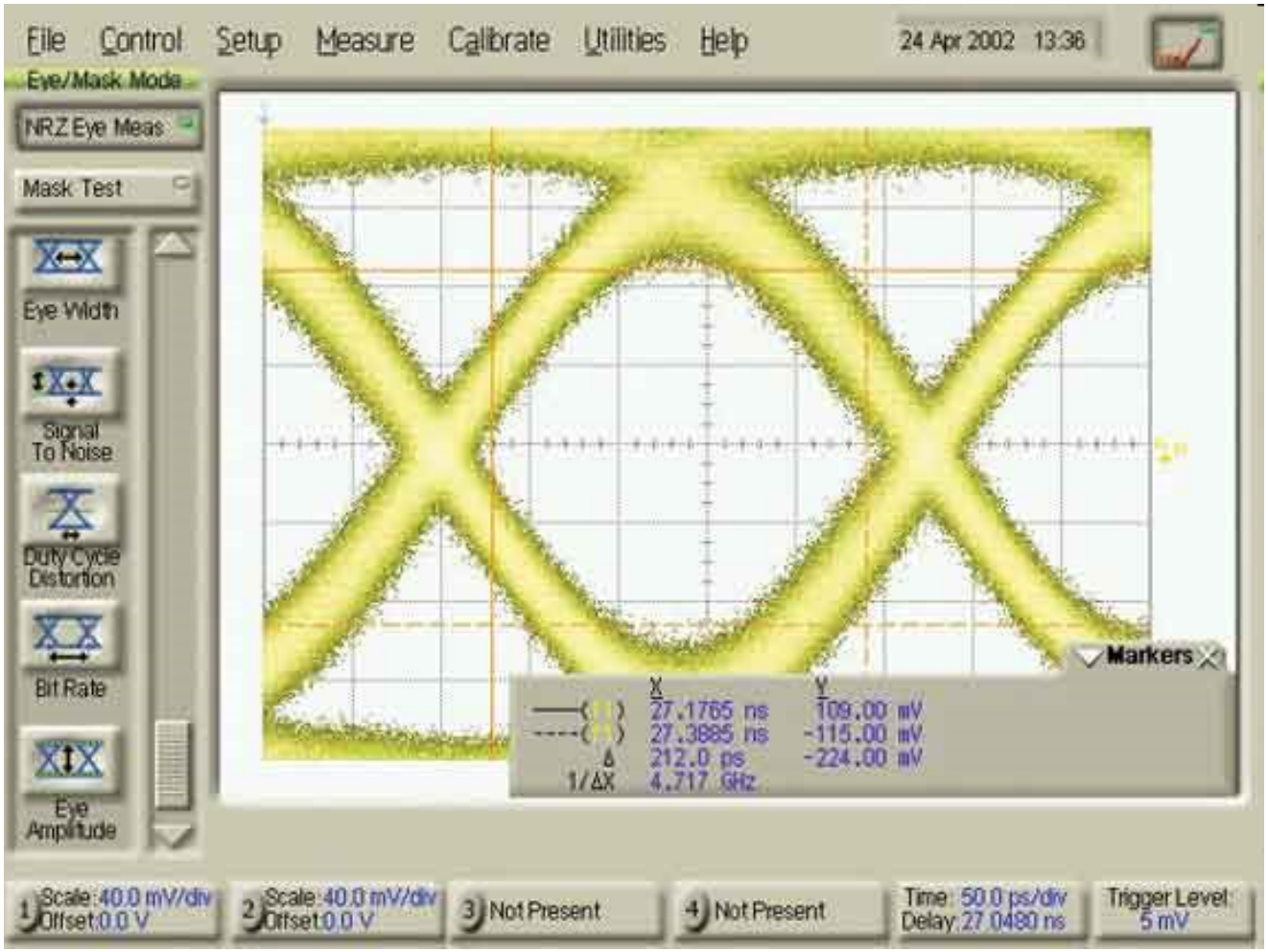
- Serdes technology is based on a serializer/deserializer pair where typical inputs, TTL signals (0 to 3.3-V swing) enter the serializer 'horizontally' and are then 'vertically' aligned so that in one clock period one set of parallel bits, or just one word, is transmitted. The internal frequency of the serializer must be faster than the incoming TTL data.

Source: Fairchild

Applications of high-speed links

- Processor to memory
- Peripherals and hard drives
- USB
- HDMI and Video
- Flash
- Ethernet backplane
- Infiniband-server backplane

Differential signals and eye diagrams



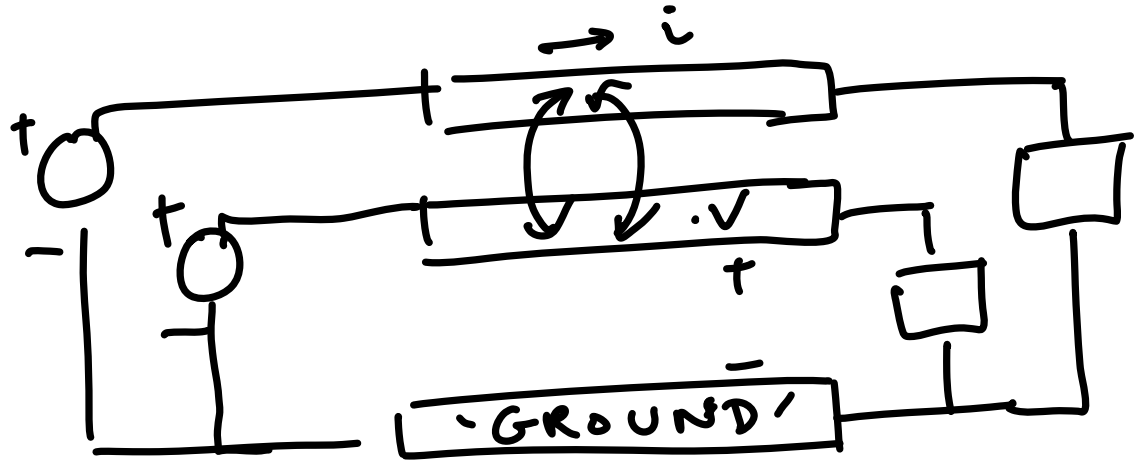
Eye diagrams

- Eye is produced by multiple passes of differential (equal and opposite signals)
- Jitter: timing randomness and amplitude randomness arising due to
  - Asymmetries in a differential system
  - Thermal and noise effects
  - Crosstalk and inter-symbol interference
- LINK to an eye diagram animation on YouTube

From an SI angle, why use Serdes?

- Why would you switch from signal-ended, low-speed, multiple parallel lines to a differential, high-speed, serial line. Any issues to expect ?
- Benefits: Less crosstalk, less noise, potentially less real estate
- Challenges: Higher-speed signals imply high-frequency SI effects: dispersion, radiation
  - Some of these may be mitigated due to differential design

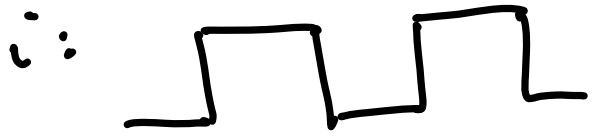
Crosstalk

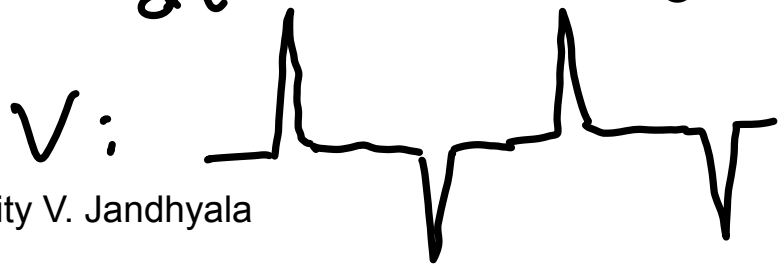


Inductive and Capacitive crosstalk

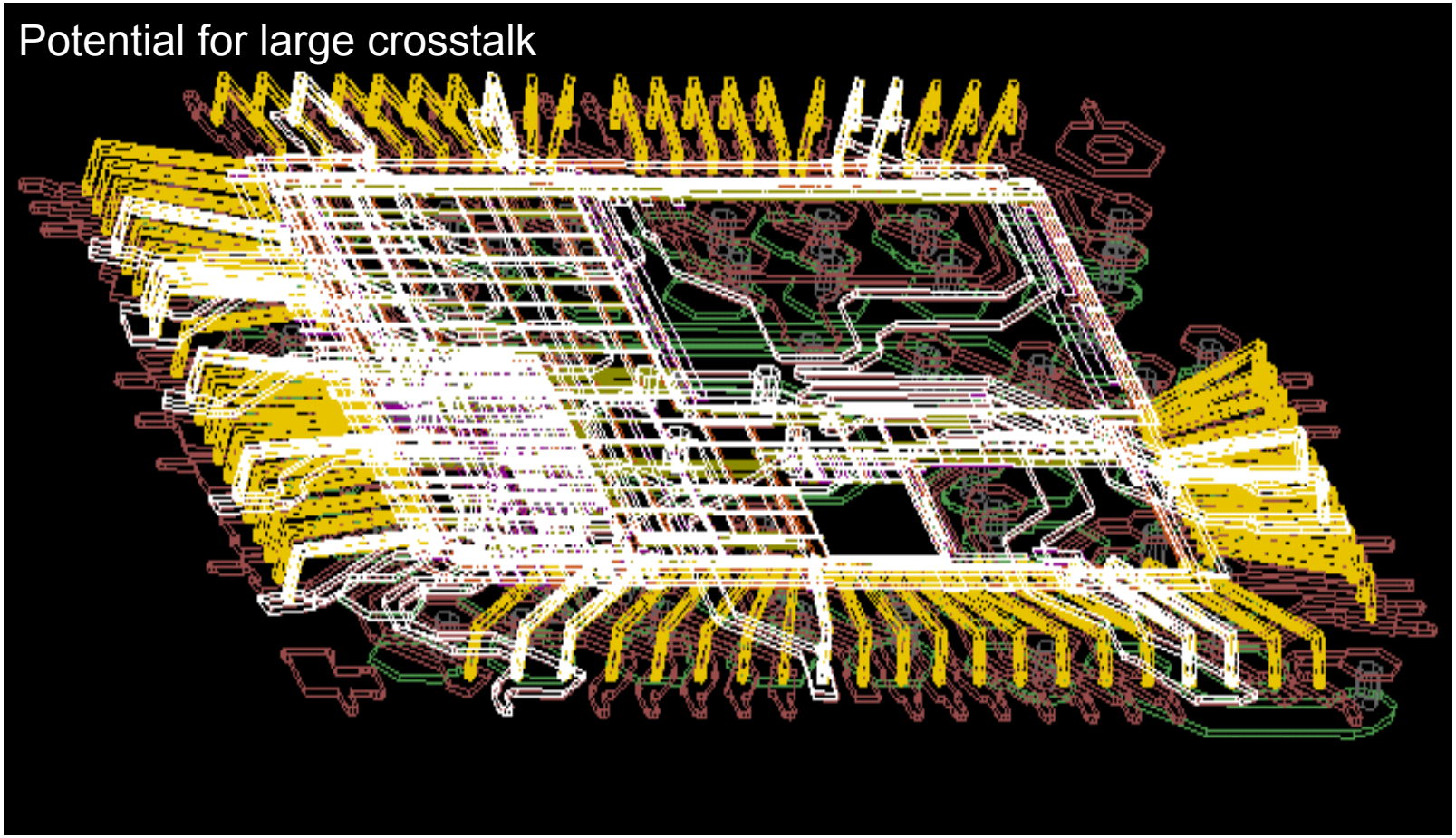
inductance (H)

$V = L\frac{di}{dt}$; $i = C\frac{dV}{dt}$



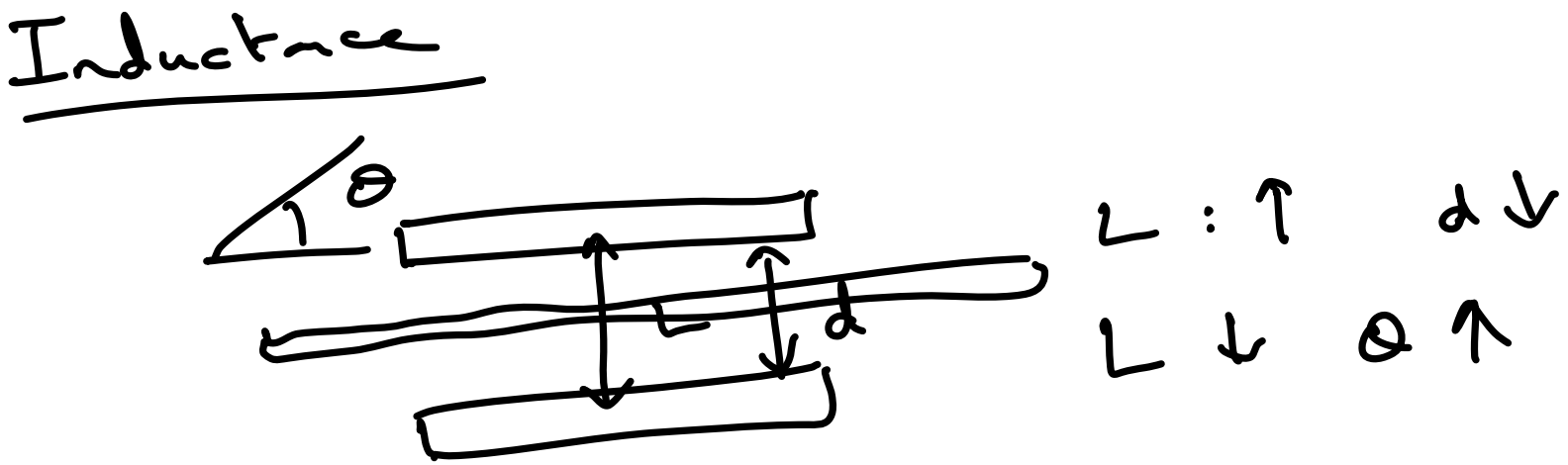


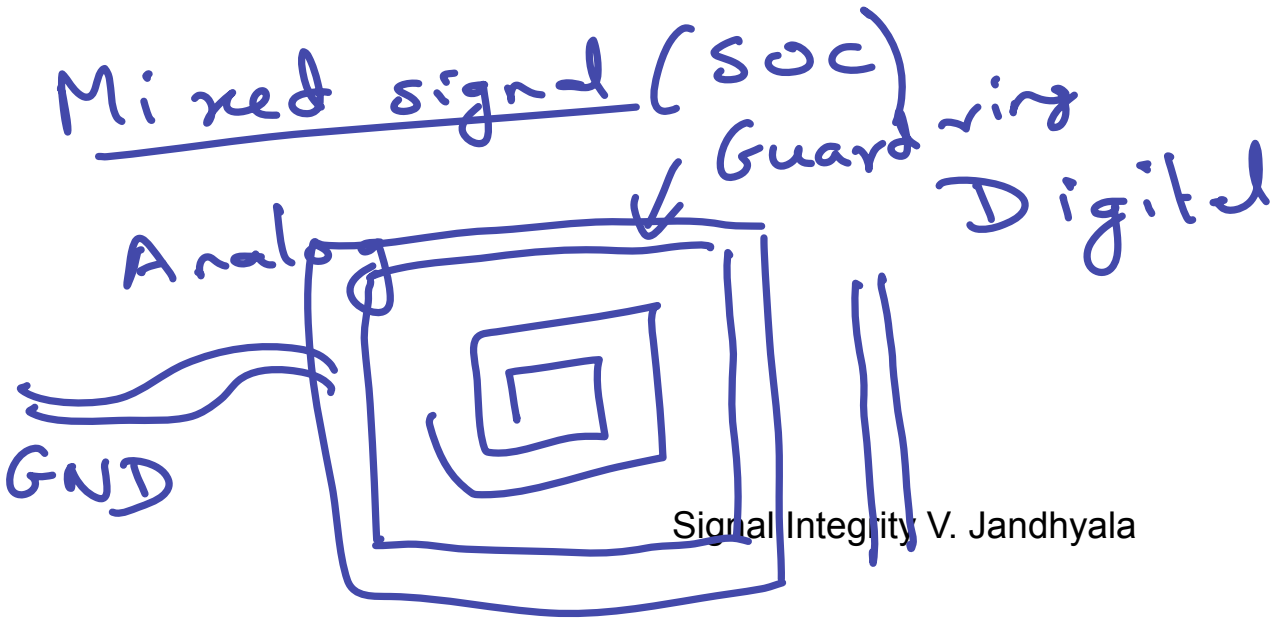
Signal paths



Courtesy: Physware

Models


Inductance
θ
d
L : ↑ d ↓
L ↓ θ ↑


Mixed signal (SOC)
Guard ring
Digital
Analog
GND

Models

:

resistor

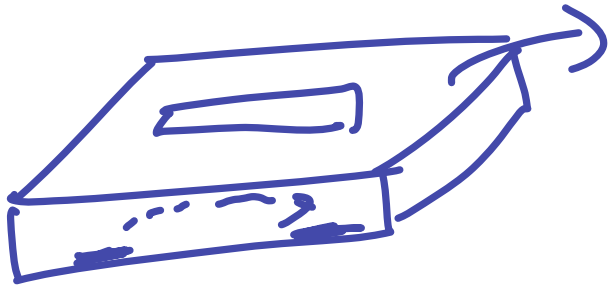
↓

models ohmic loss

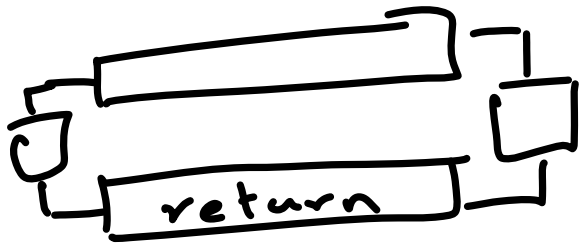
(no delay, no mismatch)

Example:

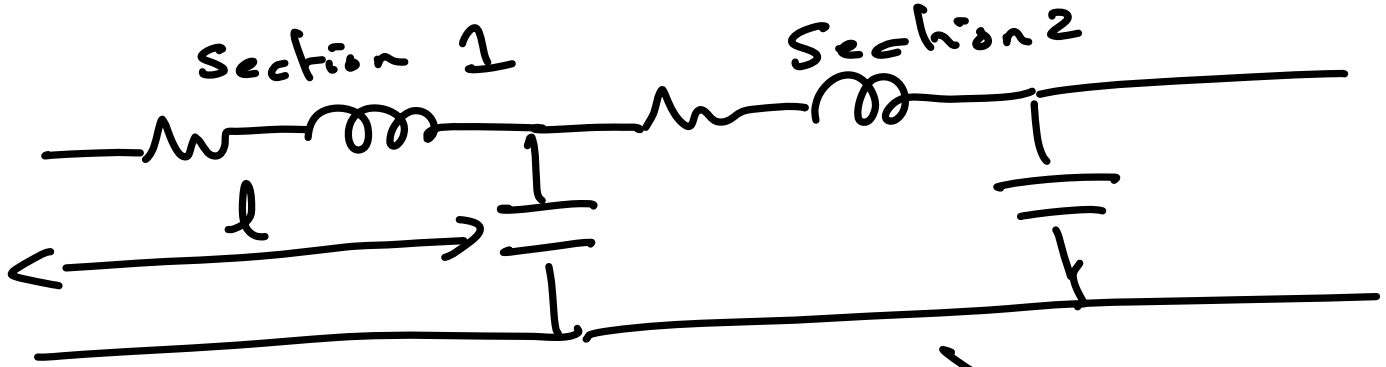
Substrate coupling (soc)



create a resistive 'mesh' of the full chip



→ Transmission line



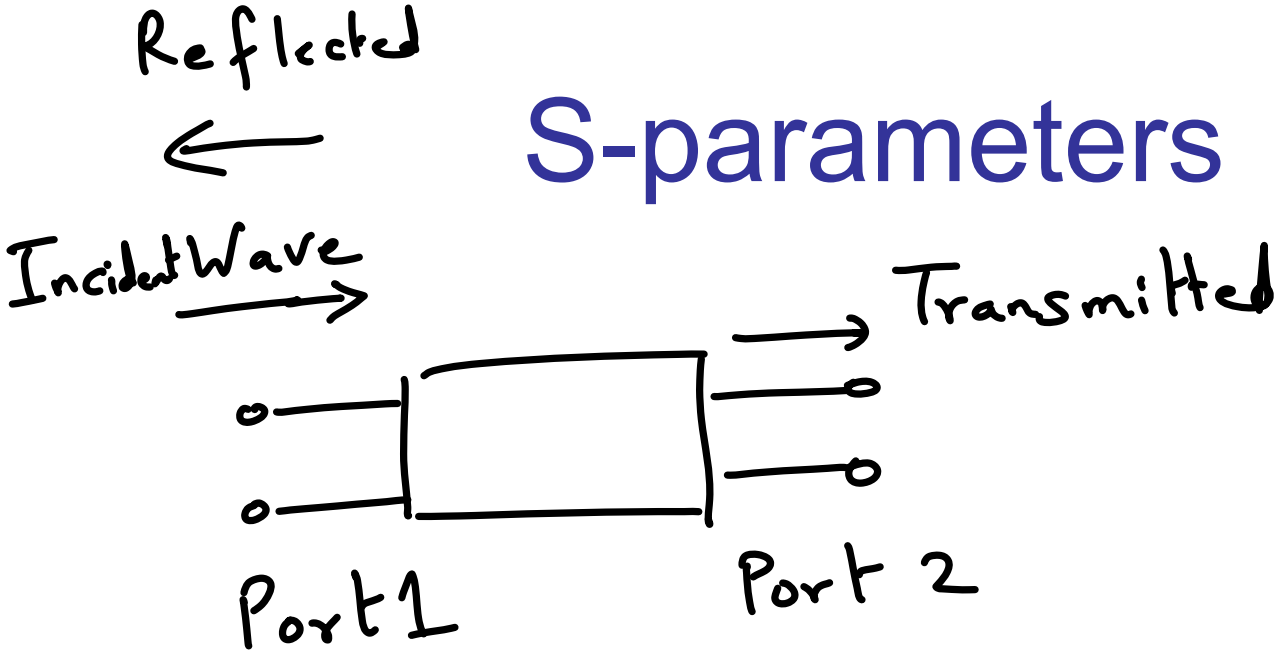
RLC ladder → Filter

Tx line:

$l \to 0$, # sections $\to \infty$

Wave equation

S-parameters



$$|S_{12}|: \frac{|\text{Transmitted}|}{|\text{Incident}|} \; ; |S_{11}|: \frac{|\text{Reflected}|}{|\text{Incident}|}$$

$$\text{Transmitted power} \propto |S_{12}|^2$$

$$\text{Reflected power} \propto |S_{11}|^2$$

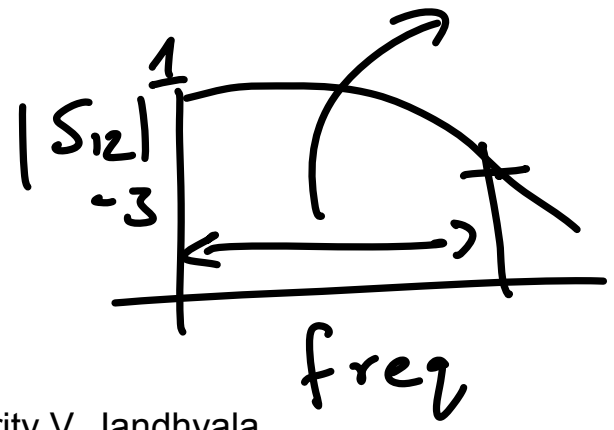
Ideally:

$|S_{11}|^2 + |S_{12}|^2 \approx 1$ + (loss)

$S_{11} = 0$ at all frequencies

$S_{12} = 1$ at all frequencies

In reality, because of material and wave/electromagnetic effects:

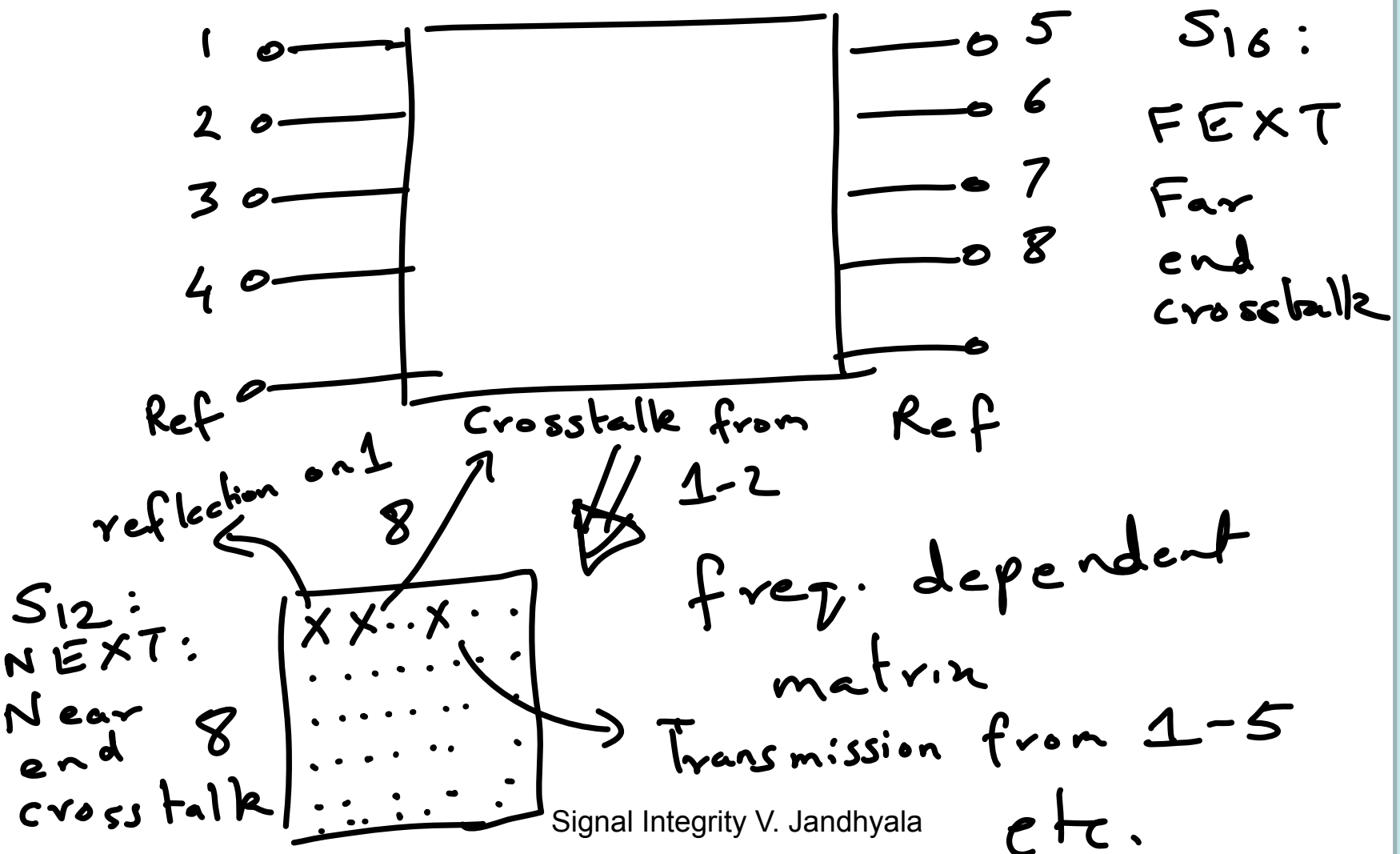


½ power BW

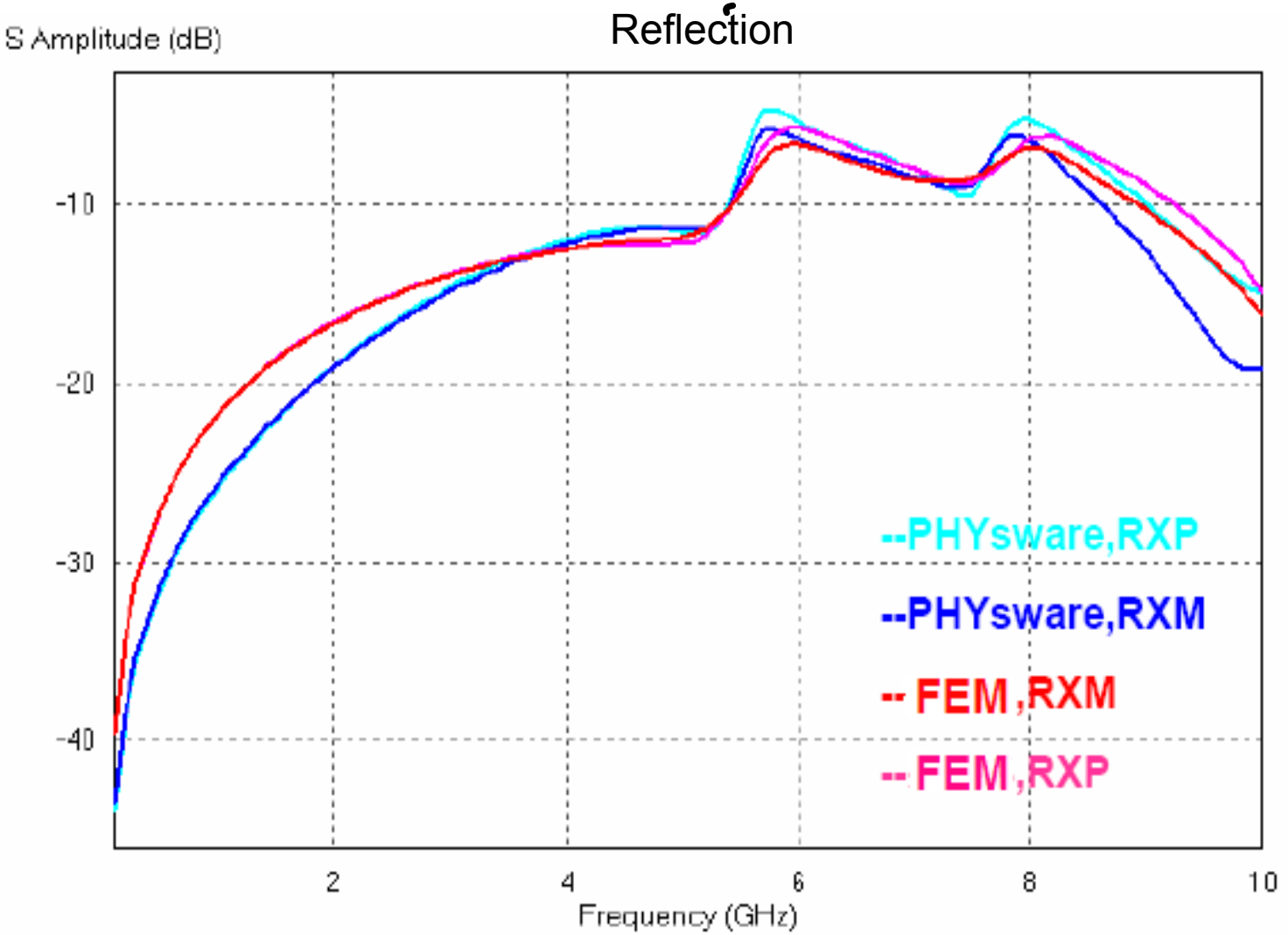
Computing S-parameters

- From lumped-circuit models
  - Z to S
  - Least accurate and easiest
- From transmission line models
  - 1D Wave equations
  - Intermediate complexity and accuracy
- From mesh-based solution to Maxwell's equations
  - 3D Wave equations
  - Most complex and high accuracy

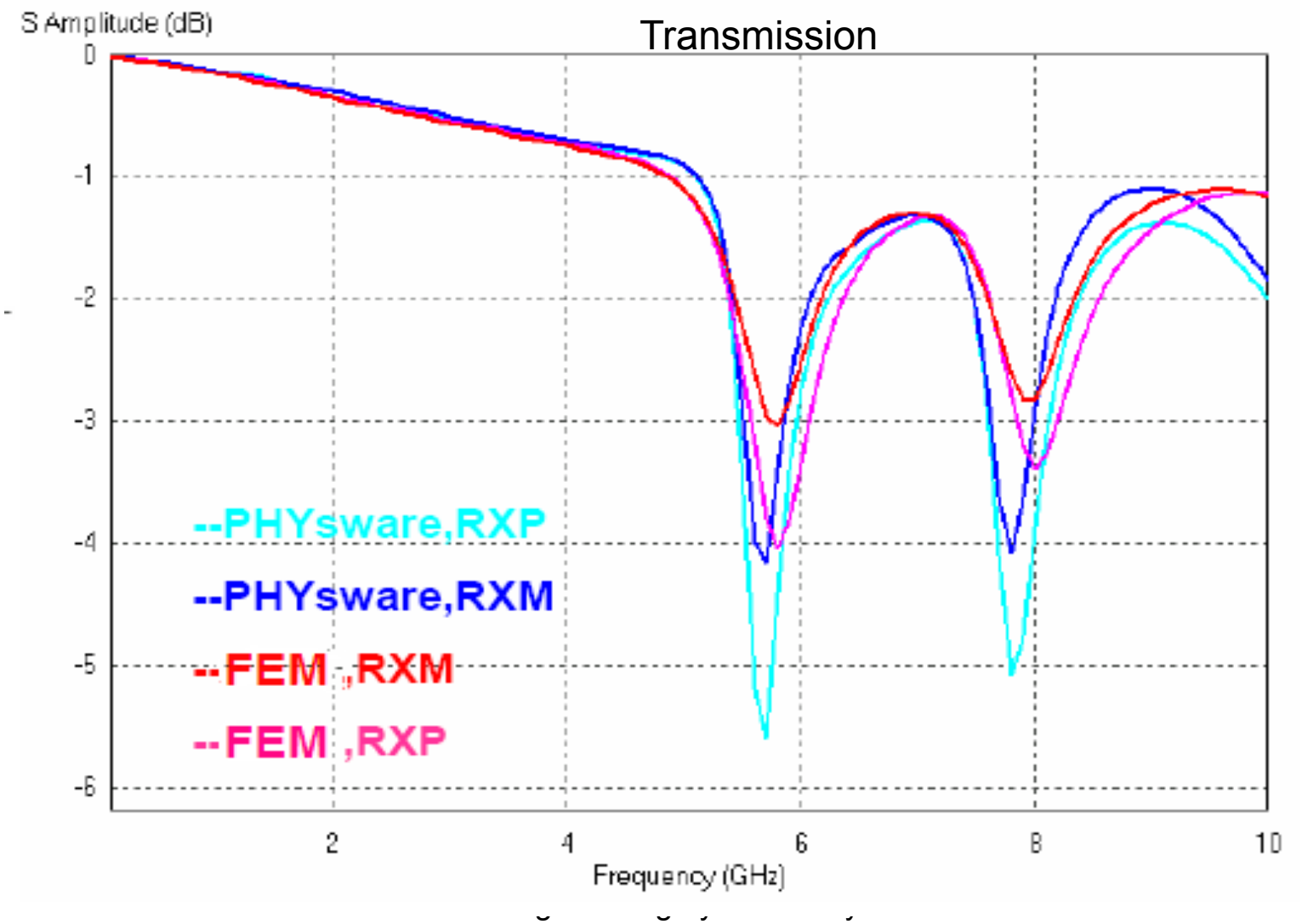
S-parameter matrix



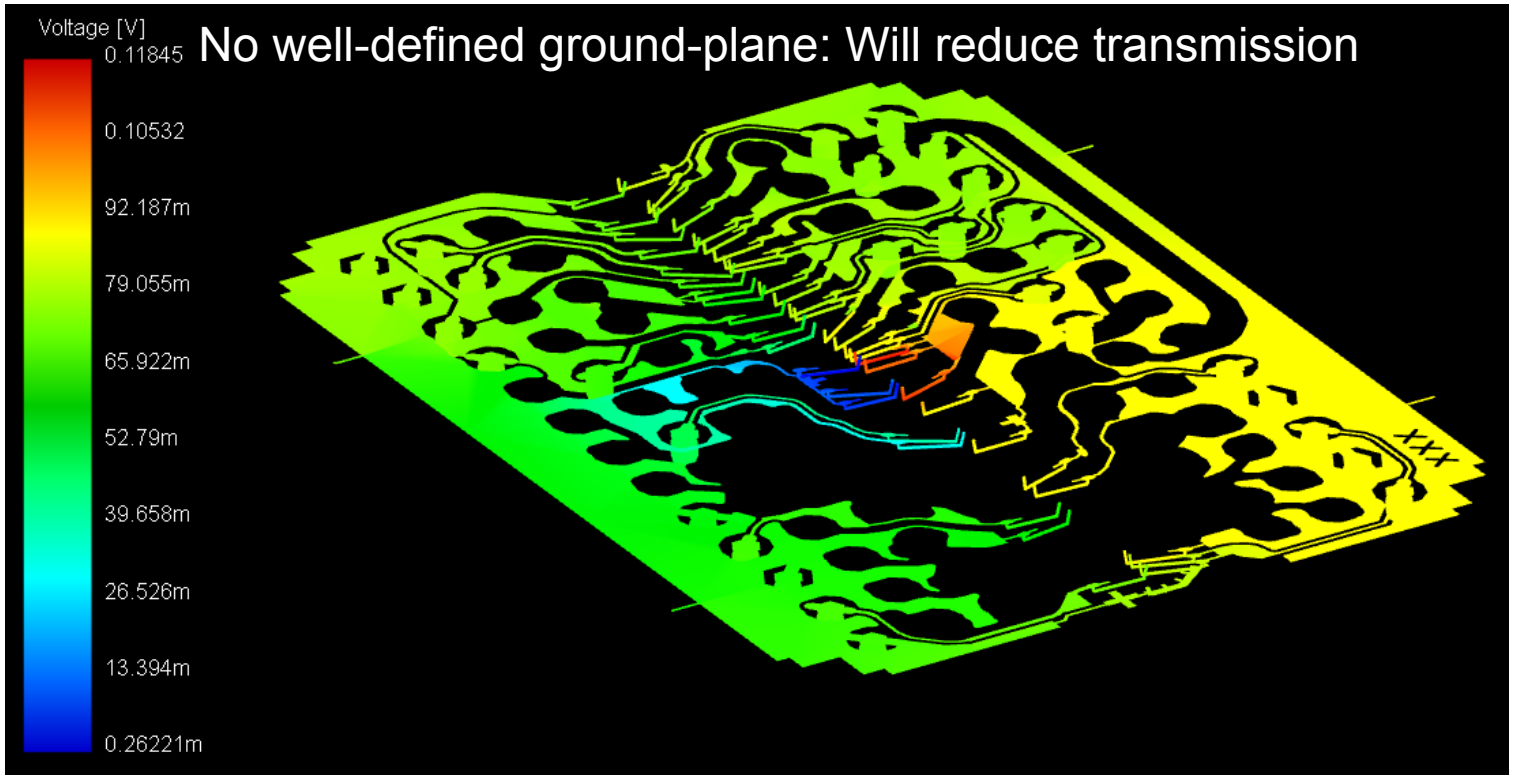
S-parameters



S-parameters

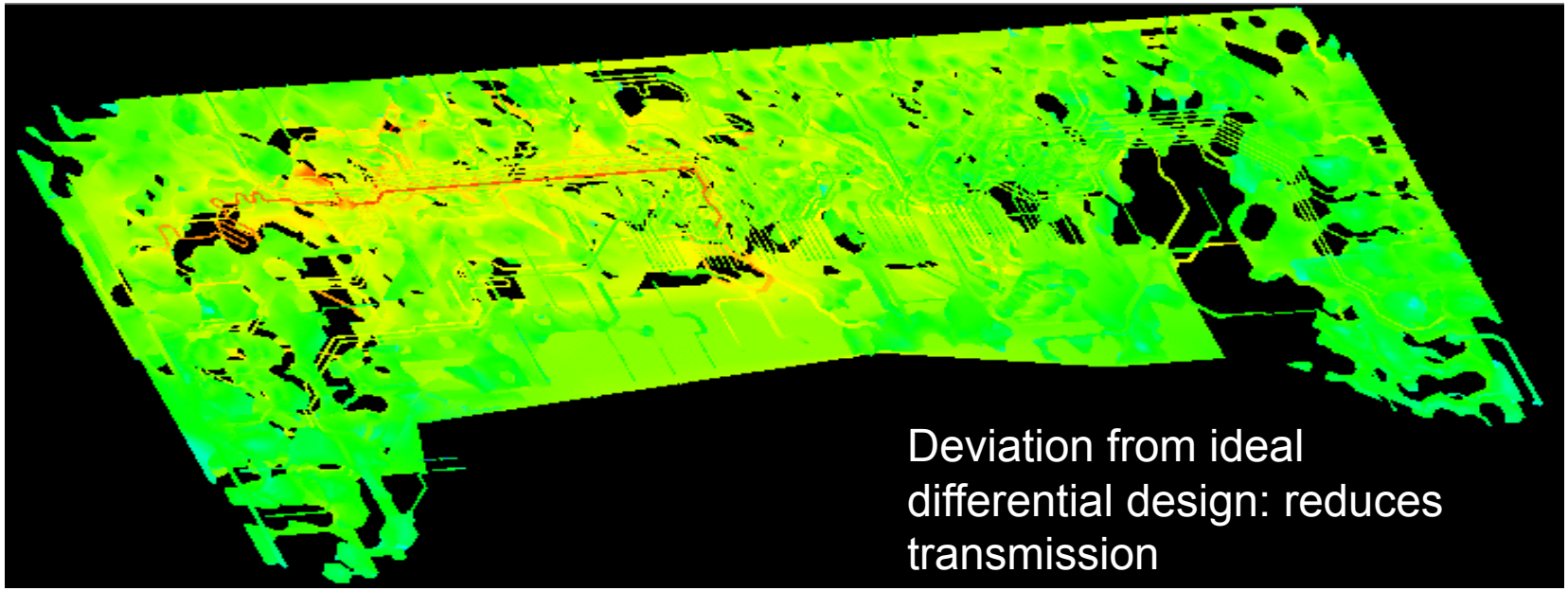


Memory



Courtesy: Physware

Return current spreading



Courtesy: Physware

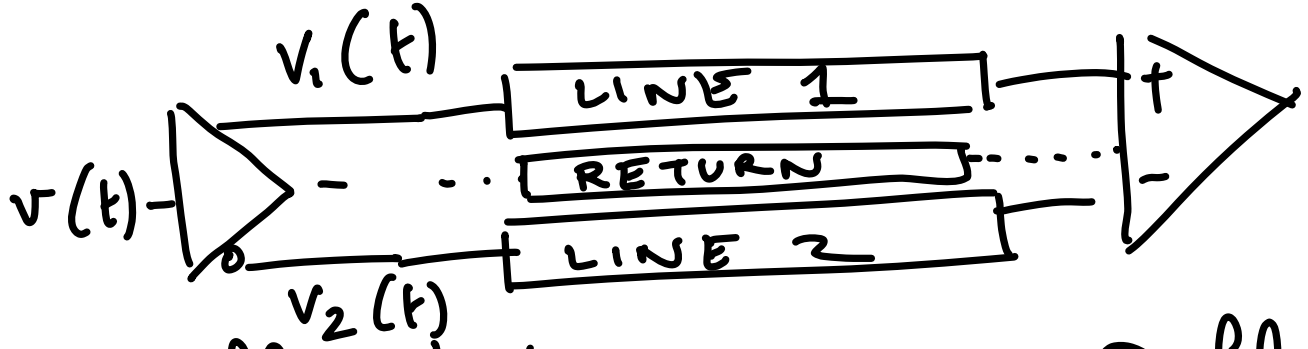
Differential signaling

Basic idea:

Send 2 signals on two lines:

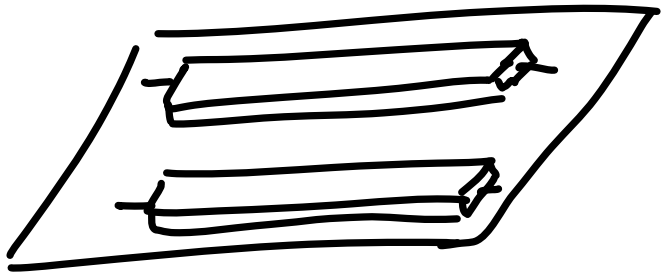
- a bit sequence
- its complement

Work with the difference of the two signals at the output



Differential driver

Differential receiver



Diff. amp measures/amplifies

$$V_{diff} = V_1 - V_2$$

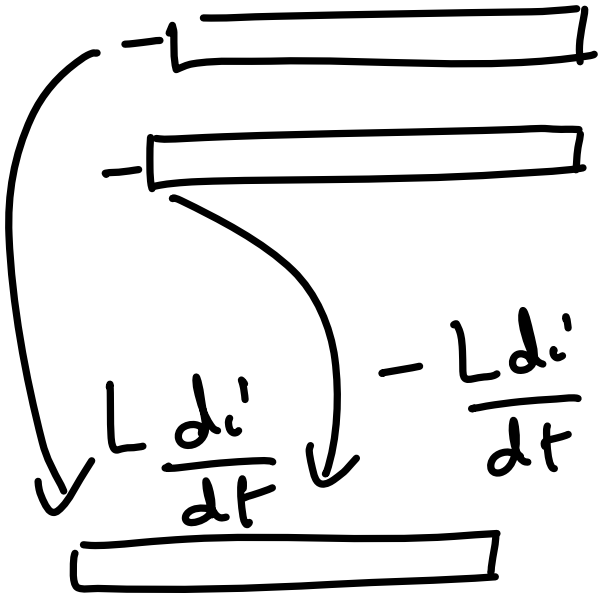
Asymmetries in the channel also create a 'common mode' signal : $V_1 + V_2$

A good differential amplifier/ receiver 'rejects' the common mode, reconstructing only the signal

CMRR : Common Mode Rejection Ratio

Benefits of diff. signaling:

1. Lower $L\frac{di}{dt}$ noise from driver injection



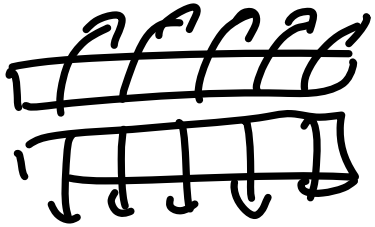
nearly cancels

2. Higher gain/amplification with low noise possible (diff. amp.)

Benefits

3. Lower voltage signaling (LVDS) due to gain

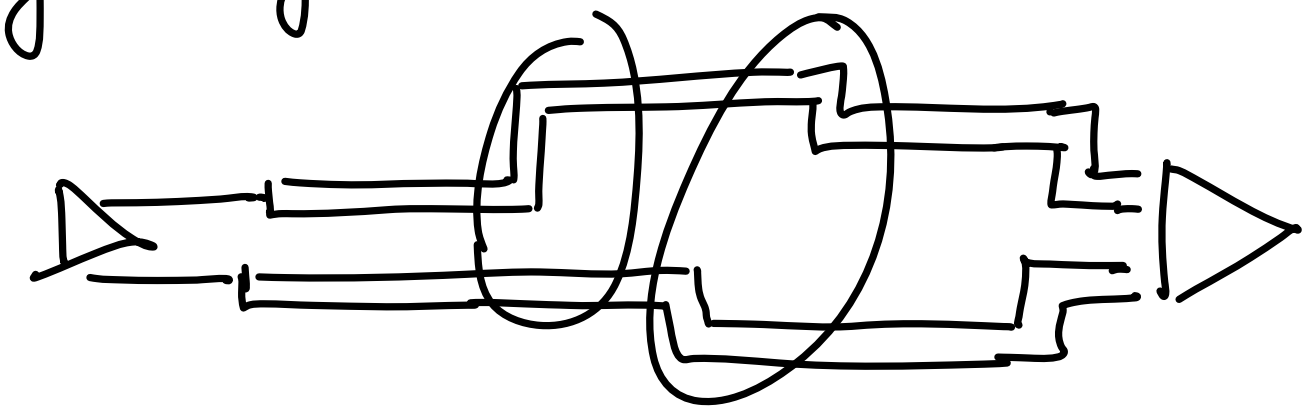
4. Lower radiation/EMI due to cancellation.



There are some negatives...

Negatives

- More signal paths / more area
- More complex drivers, receivers, and design.
- Asymmetry can lead to EMI



Sources

- EE 571 Notes Vikram Jandhyala
- Bogatin: signal integrity, Prentice Hall
- Young: Digital signal integrity, Prentice Hall
- www.physware.com
- http://www.altera.com/products/ip/dsp/images/lvds-tx-rx-ip-blockdiagram.gif
- http://i.cmpnet.com/eet/news/03/january/SS1254_FAIRCHILD.gif
- http://www.latticesemi.com/images/img12682.jpg
- http://www.youtube.com/watch?v=my7CI84le5g