Calculating the Cost of Branches

Factors to consider:

- branch frequency (every 4-6 instructions)
- correct prediction rate
  - 1 bit: ~ 80% to 85%
  - 2 bit: ~ high 80s to 90%
  - combined branch prediction: 95%
- misprediction penalty
  Alpha 21164: 5 cycles; 21264: 7 cycles
  UltraSPARC 1: 4 cycles
  Pentium Pro: at least 10 cycles, 15 on average
  - then have to multiply by the instruction width
- or misfetch penalty:
  have the correct prediction but not know the target address yet
  (may also apply to unconditional branches)

Calculating the Cost of Branches

What is the probability that a branch is taken?

Given:

- 20% of branches are unconditional branches
- of conditional branches,
  - 66% branch forward & are evenly split between taken & not taken
  - the rest branch backwards & are almost always taken

Calculating the Cost of Branches

What is the contribution to CPI of conditional branch stalls, given:

- 15% branch frequency
- a BTB for conditional branches only with a
  - 10% miss rate
  - 3-cycle miss penalty
  - 90% prediction accuracy
  - 4 cycle misprediction penalty

BTB result	Prediction	Frequency (per instruction)	Penalty (cycles)	Stalls
miss	--	.15 * .10 = .015	3	.045
hit	correct	.15 * .90 * .90 = .121	0	0
hit	incorrect	.15 * .90 * .10 = .013	4	.052
Total contribution to CPI				**.097**

Dynamic Branch Prediction, in Summary

Stepping back, how do you figure out what is important about dynamic branch prediction (or any other part of a processor)?

Prediction Research

Predicting variable values

Predicting load addresses

Predicting many levels of branches