## Today's Pipelines

Major parts of the **microarchitecture** (hardware organization)

- instruction fetch & branch prediction
- decode, register dependence analysis
- register read & instruction issue/dispatch
- integer, floating point & memory access instruction execution
- instruction reorder & commit



## 21164 Instruction Unit Pipeline

**Fetch & issue**

- instruction fetch, decode, issue
- branch handling
- instruction prefetching
- hazard detection, forward or stall
- interrupt handling

**S0**: instruction fetch
branch prediction bits read

**S1**: opcode decode
target address calculation
if predict taken, redirect the fetch
instruction TLB check

**S2**: instruction slotting: decide which of the next 4 instructions can be issued

- intra-cycle structural hazard check
- intra-cycle data hazard check

**S3**: instruction dispatch

- inter-cycle load-use & WAW data hazard checks
- inter-cycle structural hazard check
- register read

## 21164 Integer Pipeline

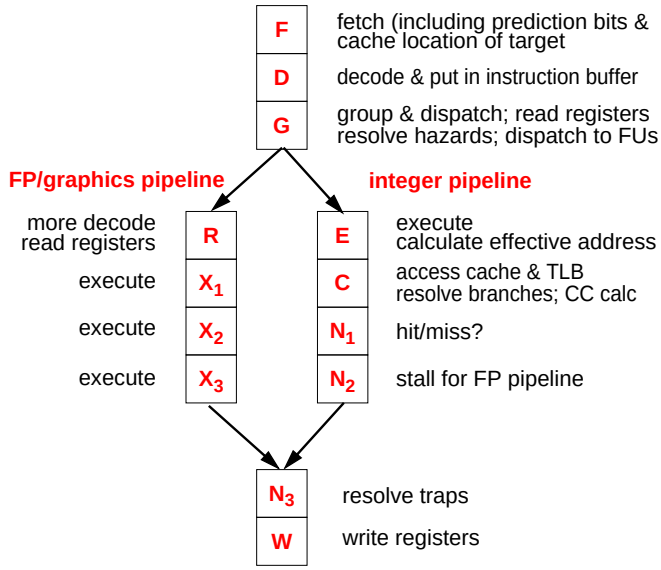
**Execute** (2 pipelines)

- also a 9-stage FP pipeline
  - **S4**: integer execution
    effective address calculation
  - **S5**: conditional move & branch execution
    data cache access
  - **S6**: register write



## UltraSPARC-1

**Integrated integer & (partial) floating point pipeline**



## UltraSPARC-3

A: generate & transmit instruction fetch address
P: 1st instruction fetch cycle
1st branch prediction cycle
F: 2nd instruction fetch cycle
2nd branch prediction cycle
B: 1st decode cycle
calculate branch target
I: 2nd decode cycle
put instructions into instruction queue
J: steer instructions to functional units
R: read source operands from register file
check operand dependences

F
D
G



## UltraSPARC-3

E: execute integer instructions
1st data cache access cycle
read FP registers
C: 2nd data cache access cycle
1st FP execution cycle
M: special cycle for half-word & byte loads
2nd FP execution cycle
W: write speculative integer register file
3rd FP execution cycle
X: extend integer pipeline to match FP pipeline
4th FP execution cycle
T: report traps
D: write real register file

E
C
$N_1$
$N_2$
$N_3$
W