Testing and Debugging

- Logic Probe very simple but enough for quick test
- Oscilloscope
 - Shows electrical details
 - Benefits: Wideband, accurate
 - Disadvantages: < 4 inputs; triggering</p>
- Logic analyzer
 - \Rightarrow Shows 0/1 according to some threshold
 - Benefits: Many channels, trigger on patterns
 - Disadvantages: Idealized waveforms, insufficient access
- ♦ 3. Embedded test
 - → You design in built-in test features
 - Benefits: Only way to test large chips
 - Disadvantages: Uses chip area, incomplete scan, difficult design

Logic Probe

Examine one signal

- ⇒ Display 0/1/Z/changing
- Select TTL or CMOS technology (5v)

Catch pulses

- ✤ Connect to signal, set pulse
- ✤ If pulse occurs, probe triggers and catches it
- Very rudimentary, but quick to catch simple things
 - Unconnected signals (bad protoboard, broken wire)
 - ↔ Wrong connections
 - ➡ Bad chips

Oscilloscope

Samples signal voltage over time

 \Rightarrow Displays signal as a waveform, one voltage value per time step \setminus

Triggering

- Choose when to start sampling the signals
- Slope: rising voltage/falling voltage
- Threshold: trigger when signal reaches this value

Repeat mode

- Assume that signal is periodic
- Repeated triggering captures the same signal
- ♀ You'll never see a glitch

Capture mode

- Triggers only once, stores waveform in memory
- ♀ You'll be very lucky to catch a glitch

Logic analyzers

Instruments for acquiring digital data

- ✤ Wide data "bus" capture many signals
- Memory stores bus data
- Smart triggering decides what data to store
- Embedded computer processes the data

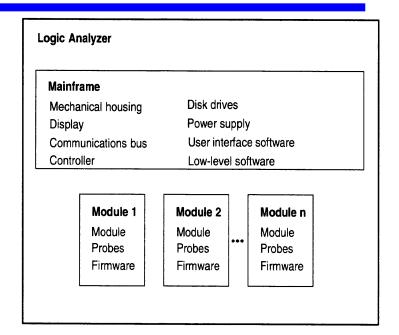
We use the Tektronix TLA704

- ⇒ 128 channels
- ⇒ 32k memory per channel
- ⇒ 100MHz state
- ⇒ 2GSPS sampling
- ⇒ Win95 interface

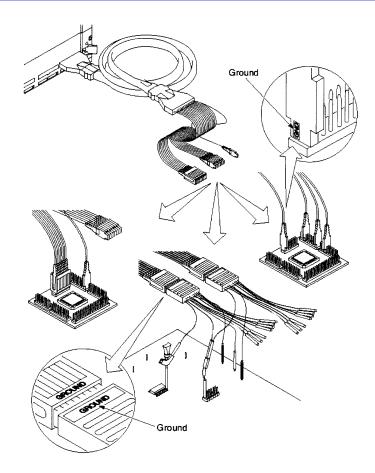


Logic analyzer physical model

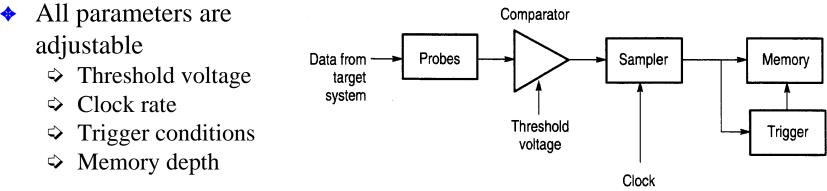
- ♦ A mainframe
 - ↔ Housing, bus, controller, UI
- Plug-in modules
 - Modules acquire data
 - - ♦ 32k memory depth
 - ♦ 100MHz state
 - ♦ 32 data and 2 clock each
- Probe pods
 - Pods are wire bundles
 - Probes attach to your circuit
 - We have P6417 probes

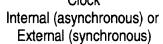


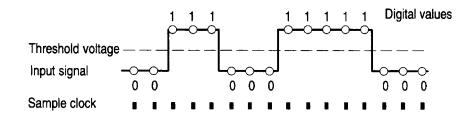
Probe pods



Logic analyzer conceptual model



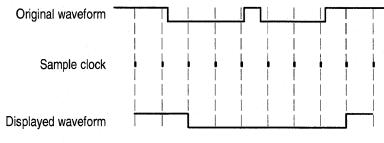




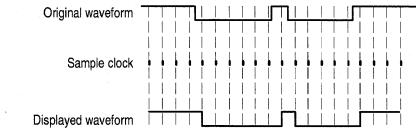
Clocking a logic analyzer

- Samples data every clock cycle
- External/synchronous clocking
 - \Rightarrow You supply the clock
 - Use when you need to see long data records
 - Analyzer stores one sample per clock period
- Internal/asynchronous clocking
 - \Rightarrow Analyzer supplies the clock
 - 4ns to 50ms
 - Use when you need to see precise timing
 - Find glitches

Example 1: Slow sample clock



Example 2: Fast sample clock



Triggering and acquisition

Derive trigger from sampled data

- Data values
- Data ranges
- Signals from another module
- Internal counters

Data acquisition is continuous

- Memory is a circular buffer
- New samples continually overwrite oldest samples
- Trigger tells the acquisition to stop

Triggers can qualify acquisition

✤ Store only selected data

Modules are semi-autonomous

Each module has its own setup

- \Rightarrow Its own clock
- → Its own trigger
- Acquires and stores its own data

Modules communicate via their trigger programs

- Can trigger all modules
- \Rightarrow Or have one module arm another
- All data is time correlated
 - Regardless of the module

System window

- Top-level in hierarchy
 - \Rightarrow Open other windows
 - Module
 - Data
 - Create new data, listing, and waveform windows
 - Shows which modules are associated with a data window
 - Enable/disable modules
 - \Rightarrow Save and load files



Displays Status

Monitor

*Note: We don't have DSO modules

Logic analyzers

Selects Repetitive or

Single-run mode

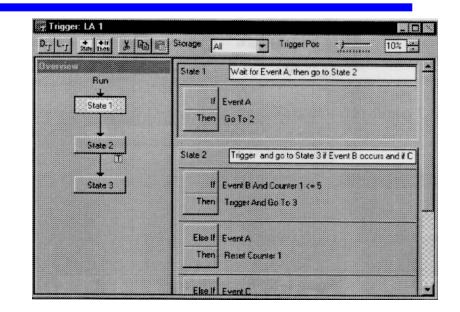
Module setup window

- Each module has its own setup and trigger windows
 - Set up each module independently
- Set all parameters
 - \Rightarrow Assign channels to groups
 - \Rightarrow Thresholds
 - \Rightarrow Clock rate
 - ✤ Comparisons
- Configure setup before trigger
 - Trigger settings depend on the module settings

Clocking. Acquire:	Internal Normal	4ns		Hemory De Support Par		68 Ione		how Activity
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A2	(7-0)	A2(7-0)						¢z
			Probe Cha	nnels / Na	mes			
Probe	7 6	5	• 4	3 ****	2	1	0	CLKQual
• A2	• •							X
A1								CK1
A0								
D3								QO
Not gro	cted group ouped r group(s)	Table Shows	Channe	ed Group el Polarity el Compare			Defi	ne Compare

Module trigger window

- Triggering is the *key* feature of a logic analyzer
 - Tells the analyzer how to find the data that you want
 - Trigger off a data pattern
 - Trigger off a data sequence
 - ↔ Multiple states
 - Multiple clauses per state
- Analyzer has a trigger library!
- Logic analyzers are designed for non-repetitive data
 - Unlike an oscilloscope



Data windows

- Many types
 - ⇔ Listing window
 - ⇔ Waveform window
 - ↔ Histogram window
 - Source-data window
- Features common to all

 - → Flags
 - → Scroll
 - ⇒ Search

-562.500 ns FT607D2A 0000 8FC7 1C -187.500 ns FT607D2C 7000 8FC5 1C 9 ps FT540000 5555 AFCF 1E 375.000 ns FT607D2C 3007 8FC4 1C 1.125,000 us FT607D32 4EB9 8FC7 1C 1.500,000 us FT607D32 4EB9 8FC7 1C 1.500,000 us FT607D34 0060 8FC7 1C 2.5250,000 us FT607D34 0660 8FC7 1C 2.625,000 us FT607D34 0660 8FC7 1C 2.625,000 us FF607D36 41AA 8FC7 1C 3.000,000 us FF607D38 2E1F 8FC5 1C 3.375,000 us FF00620E 060 AF9F 1E 2.71LA1: Sample 494.000 ns F 500 500 2.71LA1: A2(7) 2.71LA1: A2(7) 2.71LA1: A2(4) 494.000 ns 500 2.7.1LA1: A2(4) 494.500 ns 500 500 500 500 2.7.1LA1: A2(4) 491, 500 ns	: 68340 1942	<u> </u>	C2. My 61	8340	1946		1	
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AA

Capturing glitches

- Trigger on the glitch
 - Triggering looks for multiple transitions in a clock cycle
 - Captures dynamic hazards
- Can also trigger on setup and hold violations

C1: -14.8ns	C211.8ns		Delta Time: [3ns	4	
alyzer: Mag_Sample C1:		C2.		Delta		
	02	J				
yze: Mao Sample -34.50	0 25				47.	900 jus
vzer Meg. FF-CLK						
naluzen Maga Elsik		ļ 📋				
salyzer Mag FF-Q		<u></u>				
veer FF 0.001100			. i			

Other features: Activity indicator

- How do you know if a pod is active?
 - ↔ Hooked up properly?
 - Seeing data?

			Close
СК0 _	A3(7-0)	A2(7-0)1111 _	Help
СК1 🔔	A1(7-0)1111	A0(7-0)1111	
Q0 -	D3(7-0)1111	D2(7-0)1111	7 <u>-</u>
СК2 🔔	D1(7-0)1111	D0(7-0)1111	5
СКЗ 🔔	C3(7-0)TITT	C2(7-0)	4
Q1 🔔	C1(7-0)1111	CO(7-0)	3
03 _	E3(7-0)TIII	E2(7-0)	2
Q2 -	E1(7-0)1111	E0[7-0]	0

Other features: Programmability

- Symbols
 - ♀ You define in a LUT
 - Analyzer assigns symbols to data patterns
- User programs
 - e.g. export to file and continue

		Time/Div: 20	Ons 💌 Rull I L
C1: Os	2 50ns	······································	Firmes 50ns
Address	C3FFE4	Х сзре	26 X 001572
Data	NMI_7	IPL_	6 NMI_7
Control	DATA_SP		PREFETCH?

Other features: µP support

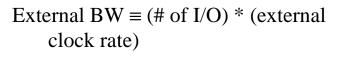
- Analyzer disassembles data to µP mnemonics
- Requires special module podsets

1 + <u></u>	HE Coto	A A	A m + Code						
: 68340									
3 ample	CPU92 Address	CFU32 Data	CPU32 Minemonic		Timestaup				
0	0000130C	0000	(READ)	(3)	-37.529,000 t				
1	0000130E	0005	(READ)	(3)	-37.154,000 1				
2	0050431E	5380	3UBQ.L #1.D0	(3)	-35.779,000 1				
3	00504320	4480	TST.L DO	(3)	-35.404,000 1				
4	00504322	5EEE	BGT.B 00504012	(3)	-35.029,000 1				
5	00504324	5381	(FLUSH)	(3)	-35.654,500 1				
6	00504312	OCB9	CMPI.L #00000007,000	01300 (3)	-35.279,500 1				
7	00504314	0000	(EXTENSION)	(3)	-34.904,000 1				
8	00504315	0007	(EXTENSION)	(3)	-34.529,000 1				
9	00504318	0000	(EXTENSION)	(3)	-34.154,500 1				
10	00504318	130C	(EXTENSION)	(3)	-33.779,500				

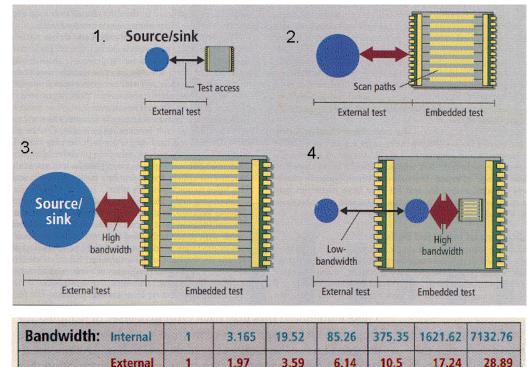
Testing: The big picture

- The difference between internal and external BW has driven test technology
 - 1. External test
 - 2. Embedded scan path
 - 3. High-BW embedded
 - 4. Embedded source

5. ???



Internal BW \equiv (# of transistors)* (internal clock rate)



From IEEE Spectrum, 7/99, pgs. 55 / 57

1997

1999

2002

'05

'08

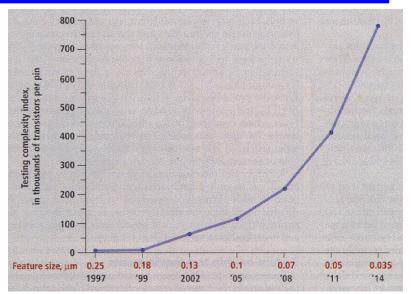
Source: 1998 International Technology Roadmap for Semiconductors

'14

'11

Semiconductor scaling confounds testing

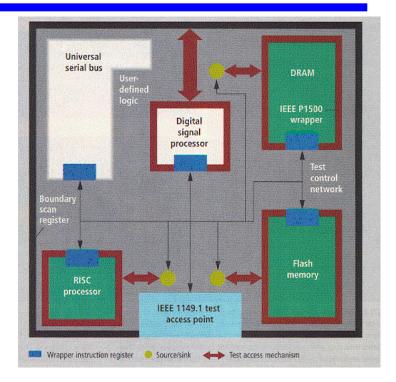
- Testing is a key obstacle to future advancement in digital technology
- Need to ensure logic functionality
 - Despite ever-more-limited access to internal logic
- Testing at the board, subsystem, and system level becomes ever harder



From IEEE Spectrum, 7/99, p. 55

System-on-a-chip testing

- IEEE P1500 standard
 - \Rightarrow For embedded core test
 - \Rightarrow In development
- Standardized core test language
- Standardized core test wrapper
 - ↔ Configurable
 - ♀ Scalable



From IEEE Spectrum, 7/99, p. 59