What is pipelining?

- Overlapping Execution of instructions
- Temporal parallelism
- Instructions in different phases of execution

- Multiple instructions in flight
- Simultanious use of hardware
- Aim: High clock rate through parallelism

Why is it good?

- Higher clock rate, leading higher throughput
- Higher utilization (efficiency)
- Sometimes transparent to ISA

What makes it hard?

- Dependencies
  - Control
  - Data
    - Memory (main)
    - Registers: RAW, WAW, WAR
- Structural hazards

What are hazards?

Is there a limit to pipelining?

- Clock rate is set my maximum pipe stage delay
- Pipeline stage overhead
- Properties of the application
  - Branch Frequency & Prediction Accuracy
  - Memory I/O