CSE548

The von Neumann Execution Model

Rahul Banerjee
9th Jan 2012

Electronic Numerical Integrator And Computer

- Finally assembled in fall 1945
- Designed by John Mauchly and J. Presper Eckert for the US Army's Ballistics Research Laboratory (BRL)
- Built for speed & reliability, for computing trajectories
- Used decimal computation (ring counters)
- 3 x Function tables (basically lookup tables)
- Functioning units with local program control
- No storage, but accumulators stored 20 x 10-digits
- Synchronous (20 pulses of 10μs = 1 timing cycle)
- Vital stats:
  - ~18k vacuum tubes; ~7k crystal diodes; 1,500 relays; 10k capacitors
  - Weight 30 tons (18000 ft^2); 5M hand-soldered joints; Cost ~ $500,000
  - Consumed ~200 kW of electrical power (estimates vary)
- (Re)programming?
  - (Re)wiring accumulators, func tables, IO units...
  - By 1949, was converted into stored fixed-program computer at von Neumann's suggestion

Electronic Discrete Variable Automatic Computer

- Delivered in August 1949, but operational in 1951
- Designed by Eckert, Mauchly & von Neumann for BRL
- Used serial binary computation
- Central Arithmetic (CA), capable of + - × ÷
- Central Control (CC), for sequencing ops (like division)
- Storage capacity: 1024 x 44-bit words
- ISA: 4 digit opcode, 4x 10-digit addr (2 src, 1 dst, 1 instr)
- Conscious design decision to keep it simple (no parallelization, or folding multiple instructions)
- Synchronous (48 pulses of 1μs = 1 timing cycle)
- Vital stats:
  - 6,000 vacuum tubes; 12,000 diodes; lotsa resistors, capacitors, etc.
  - Weight 8000 kg (500 ft^2); Cost ~ $500,000
  - Consumed 56 kW of electrical power
- Reprogramming:
  - Programs could be read in from punched card to memory

Electronic Delay Storage Automatic Calculator

- Operational in May 1949
- Designed by Maurice Wilkes for Cambridge
- Heavily influenced by EDVAC (von Neumann's report)
- Used 2's complement binary arithmetic
- Mercury delay lines (memory), vacuum tubes (logic)
- 1k locations of 18 bits (17 usable)
- ISA: 5b opcode, 1b unused, 10b address, 1b data width
- Vital stats:
  - 3000 valves, 12 kW power consumption, 215 ft^2
- Reprogramming:
  - OS consisted of 31 hard-wired "initial orders", essentially an assembler for programs from paper-tape input
  - "Wheeler Jump" allowed subroutines

Points For Discussion

- Reliability prioritized over computing speed:
  - Serial design (avoiding all parallelization)
  - Derated vacuum tubes
- Design simplicity prioritized over efficiency:
  - Fixed-field opcode encoding (as opposed to expanding opcodes)
  - Storing sequencing control in a separate, dedicated memory in CC
- Though ENIAC was supposed to be general-purpose, it was actually quite difficult to repurpose it.
- Valuable lessons learned from execution:
  - Even before completing ENIAC, architects made EDVAC a stored-program design.
  - Wilkes invented microprogramming for EDSAC 2
- Cloud = external, vast repositories of programs and data

So, what's an efficient design for a "personal computer" in today's world?

- "Network Computer" / thin client (good idea, bad timing?)
- Google Chromebook