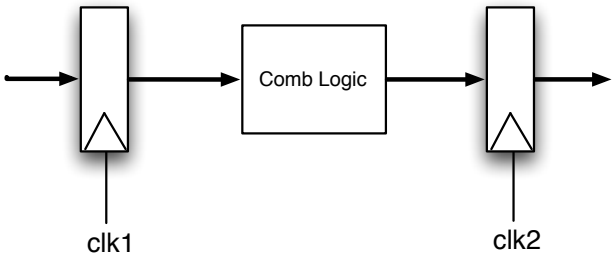
Name_____

CSE 352 – Introduction to Digital Logic Design
Autumn 2011
Homework #5 - Due 1:30, Wednesday, Nov. 16

1. Harris & Harris Exercise 3.30

The remaining questions relate to the circuit shown in the figure below. This circuit has two registers that are clocked by two clocks, clk1 and clk2. These are connected to the same "master" clock, but are each delayed by different amounts by wire delay on the clock wires. The combinational logic has a propagation delay of 700ps. and a contamination delay is 100ps. The register has a setup time of 75ps, a hold time of 50ps, a propagation delay of 150ps and a contamination delay of 25ps. The clock frequency is 1GHz.



2. Assume that clk1 is delayed by 100ps. more than clk2. That is, the clock edges happen 100ps. later on clk1 than clk2.

a) Examine the "long path" timing constraint between the two registers. Does the data make it to the second register in time, or is the clock frequency too high?

b) How much slack time is there? That is, how much longer could the propagation delay be before the circuit fails? Or if the slack is negative, how much longer does the clock period need to be? (Slack is the extra time on a path, i.e. [clock-period – critical-path-delay].)

c) Now look at the "short path" timing constraint between the two registers. Is the short path timing constraint violated? If not, how much more clock skew can be tolerated? If so, how much does the clock skew need to be reduced?

3. Now assume that clk2 is delayed by 100ps. more than clk1.

a) Look at the "long path" timing constraint between the two registers. Does the data make it to the second register in time, or is the clock frequency too high?

b) How much slack time is there? That is, how much longer could the propagation delay be before the circuit fails? Or if the slack is negative, how much longer does the clock period need to be? (Slack is the extra time on a path, i.e. [clock-period – critical-path-delay].)

c) Now look at the "short path" timing constraint between the two registers. Is the short path timing constraint violated? If not, how much more clock skew can be tolerated? If so, how much does the clock skew need to be reduced?

4. Now assume that there is no combinational logic between the registers and thus no combinational logic delay at all.

Assume that clk2 is delayed by 100ps. more than clk1.

a) Look at the "short path" timing constraint between the two registers. Is the short path timing constraint violated? If not, how much more clock skew can be tolerated? If so, how much does the clock skew need to be reduced?

b) Assume that there is no way to change the clock skew, simply because the clock wires are long. How else could you fix this circuit if the hold time constraint is violated?