

CSE 352 – Introduction to Digital Logic Design

Autumn 2011

Homework #6 - Due 1:30, Monday, Nov. 28

1. On the following page is the simple FPGA architecture discussed in class. (Note – there are slight differences, so use this one!) Use this to implement a 2-bit register with enable and reset inputs. First draw the circuit, and indicate how it is factored so that it can be placed on the FPGA. Please annotate your answer sheet as follows:

a) Label each input and output

b) In each of the mux configuration boxes, enter a 0 or 1 to indicate how you have configured the multiplexer. Use X for unused multiplexers. In addition, draw a line inside the mux from the selected input to the output. Label the selected input with the signal name assigned to that wire.

c) For each LUT, enter the 0's and 1's to show how it is programmed. Write the function that the LUT implements in the space above the LUT.

2. Implement the following function using 3-LUTs. Give the function implemented by each 3-LUT and show how the 3-LUTs are connected together. It is in your best interests to make it clear how you have implemented the function. You do **not** have to give the LUT program, only the Boolean function that it implements.

$$AB'F + ACD'F + AC'DF + A'BCF + BCDF + AEF + BCEF$$

Try to use as few 3-LUTs as possible – this is what the synthesis tools do for you every day. For example, it is pretty easy to see how to do this with 11 3-LUTs, but that's not close to the best number.

