HOMEWORK 2

Q1:

a) Harris & Harris Exercise 4.2.

(Copied for those without a book).
Sketch a schematic of the circuit described by the following HDL code. Simplify the schematic so that it shows a minimum number of gates.

The Verilog code:

```
module exercise2 (input       [3:0] a,
                  output reg [1:0] y);

  always @(*)
    if      (a[0]) y = 2'b11;
    else if (a[1]) y = 2'b10;
    else if (a[2]) y = 2'b01;
    else if (a[3]) y = 2'b00;
    else           y = a[1:0];
endmodule
```
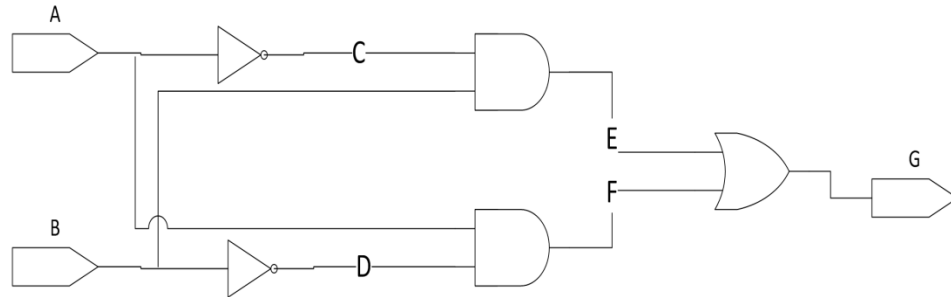
b) Harris & Harris Exercise 4.6.

Write an HDL (Verilog please) module for a hexadecimal seven-segment display decoder. The decoder should handle the digits A, B, C, D, E, and F as well as 0-9.

Make sure you denote in your comments which bits correspond to which segment, you will need this in your code. Additionally, drawing this out on a 7-segment diagram will also help as a reference when you try to code this but you don't have to turn the diagram in.

Q2:
For the circuit below, assume that all gates have the same delay (including inverters) of 5 ns, complete the timing diagrams.

	0ns	5ns	10ns	15ns	20ns	25ns	30ns	35ns	40ns	45ns	50ns
A	0	1									
B	1						0				
C	1										
D	0										
E	1										
F	0										
G	1										
Time	0ns	5ns	10ns	15ns	20ns	25ns	30ns	35ns	40ns	45ns	50ns

Q3: Complete the timing diagram for the circuit below for 10 clock cycles. Is the reset signal active low or active high?
You have learned from class that this circuit is a crucial component in sequential logic design. What is it and why do you think it might be useful?