Assignment # 6

Due Friday March 1

Read Chapter 6 Sections 1, 2, 3, and 4.
Read Chapter 7 Section 1.

1. Verilog
   - Construct a 4-bit adder as a Verilog module in DesignWorks. Use the Verilog "+" operator to implement addition. Make sure that your module includes a carry-out. Turn in your Verilog source code.
   - Connect a keypad and probes to your Verilog adder block for testing. Verify that your adder works. Turn in printouts showing the following two tests:
     - "1111" + "0001"
     - "1010" + "0101"
   - (Optional: bonus points). Turn in waveforms for the outputs for the cases above
2. Show how to implement a T-flip-flop starting with a D-flip-flop and a few gates.
3. Chapter 6 Exercise 6.12.
4. Using just basic D flip-flops and combinational logic (rather than the TTL 74194 part), design a 4-bit register that implements the shift register subsystem in Katz problem 7.3.
   - First draw a DesignWorks schematic for one cell. Feel free to use an 8:1 multiplexer in your cell design.
   - Then connect the 4 cells together.
   - Then add the external logic to handle the serial shift inputs.
   - Connect a keypad and probes to your design and verify that it works. For example, start with a sequence of arithmetic shifts to load your register with initial values. Then perform a sequence of shifts of the other categories. Turn in print-outs showing your work.