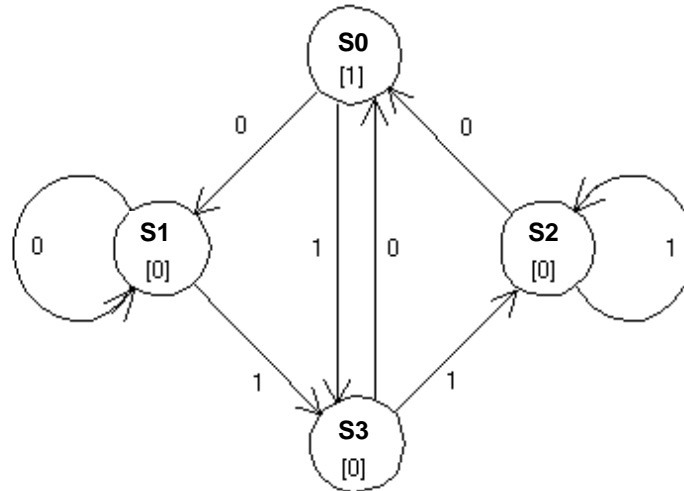# CSE370 Quiz 5 (1 December)   **Name** _____

Given the state diagram below, with single input A and single output Z, show pseudo-Verilog code (clearly identifying any assign or always blocks) that specifies the same behavior. Implement the state transitions using an always block and the output using an assign statement.


```
module state_machine (A, Z, clk);

      input A;
      output Z;

      reg [1:0] state;

      parameter S0 = 2'b00;
      parameter S1 = 2'b01;
      parameter S2 = 2'b10;
      parameter S3 = 2'b11;

      assign Z = (state == S0);  // Moore, output=fn(state)

      always @(posedge clk) begin
         case (state)
            S0: if (A) state <= S3; else state <= S1;
            S1: if (A) state <= S3; else state <= S1;
            S2: if (A) state <= S2; else state <= S0;
            S3: if (A) state <= S2; else state <= S0;
         endcase
      end

endmodule
```