

# Lecture II: Multi-Level Logic

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CSE 370, Autumn 2007  
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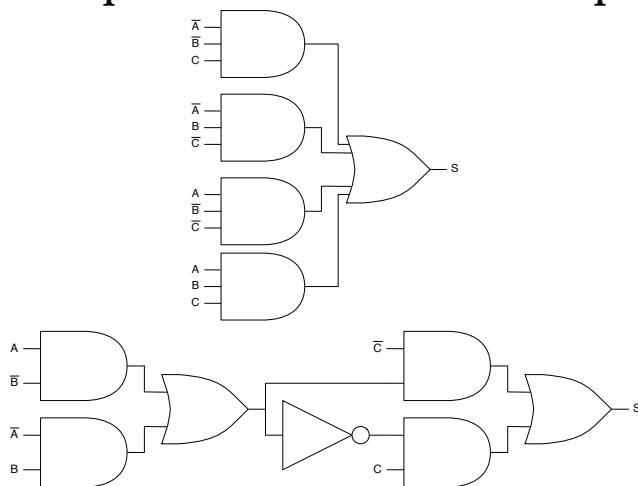
## Where We Are

- Last lecture: Quine-McCluskey Minimization
- This lecture: Multi-Level Logic
- Next lecture: Circuit Delay and Timing
- Homework 4 in progress
- Lab 3 done; lab 4 next week

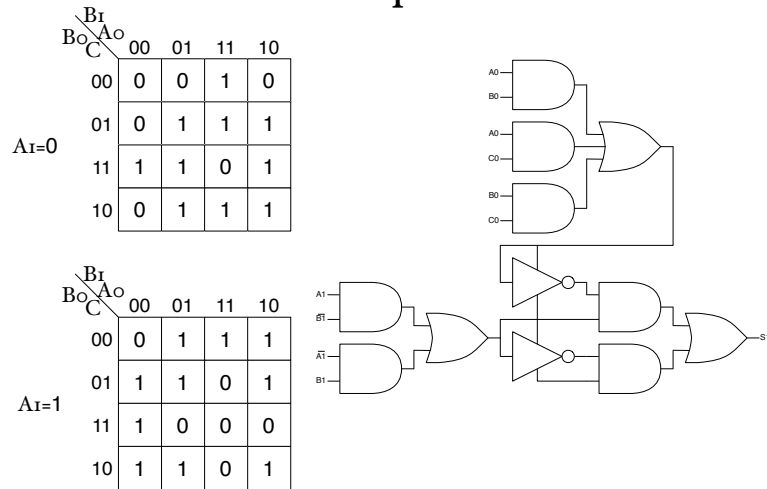
# 2-Level Minimum Circuits are Not Always the Best Solution

- Important circuit metrics:
  - Size
  - Speed
  - Complexity
  - Energy efficiency
- How we approximate these metrics:
  - Number and kind of gates
  - Number of gate inputs
  - Circuit depth

## Example: Full Adder Sum Output



## More Extreme Example: 2-Bit Adder



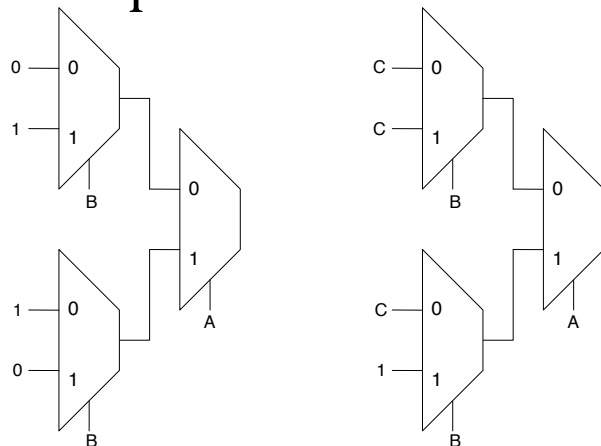
## No Simple Methods

- For 2-level minimization we have:
  - K-maps
  - Quine-McCluskey
  - Espresso
- For multi-level minimization we have:
  - Lots of heuristics
  - SIS

# Factoring

- $Z = ADF + AEF + BDF + BEF + CDF + CEF + G$ 
  - AND<sub>3</sub>: 6    OR<sub>7</sub>: 1    Depth: 2
- $Z = (AD + AE + BD + BE + CD + CE)F + G$ 
  - AND<sub>2</sub>: 7    OR<sub>6</sub>: 1    OR<sub>2</sub>: 1    Depth: 4
- $Z = (AD + BD + CD + AE + BE + CE)F + G$ 
  - AND<sub>2</sub>: 7    OR<sub>6</sub>: 1    OR<sub>2</sub>: 1    Depth: 4
- $Z = [(A + B + C)D + (A + B + C)E]F + G$ 
  - OR<sub>3</sub>: 2    AND<sub>2</sub>: 3    OR<sub>2</sub>: 2    Depth: 5
- $Z = (A + B + C)(D + E)F + G$ 
  - OR<sub>3</sub>: 1    OR<sub>2</sub>: 2    AND<sub>3</sub>: 1    Depth: 3

## Using Multiplexors to Implement Functions

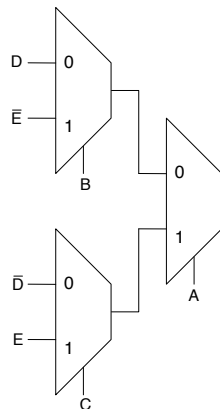


# Cofactoring

- $Z = ACE + A\bar{C}\bar{D} + \bar{A}B\bar{E} + \bar{A}\bar{B}D$ 
  - Cofactor A
- $Z = A(CE + \bar{C}\bar{D}) + \bar{A}(B\bar{E} + \bar{B}D)$ 
  - Cofactor C in the left expression and B in the right expression
- $Z = A(C(E) + \bar{C}(\bar{D})) + \bar{A}(B(\bar{E}) + \bar{B}(D))$

# Translating to Muxes

- $A(C(E) + \bar{C}(\bar{D})) + \bar{A}(B(\bar{E}) + \bar{B}(D))$



# Thank You for Your Attention

- Start reading lab 4
- Start looking at homework 4
- Continue reading the book