The challenge: perform 32-bit addition/subtraction with only a 16-bit adder/subtracter, a finite state machine, and some registers.

The design approach we will use to solve this problem: "control/datapath design"


| A | B | add/sub |  |
| ---: | ---: | ---: | ---: |
| cOnt | +/- | cln |  |
|  |  |  |  |
| Sum/Diff |  |  |  |

Challenge 2: Perform multiplication of two 8-bit numbers, with a 16-bit output, with only a 16-bit adder, shift registers and a FSM.


