Name:

CS370: Introduction to Digital Design — Instructor: B. Hemingway

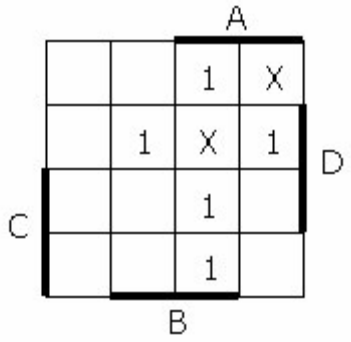
Quiz #2—Take-home version

April 30, 2007

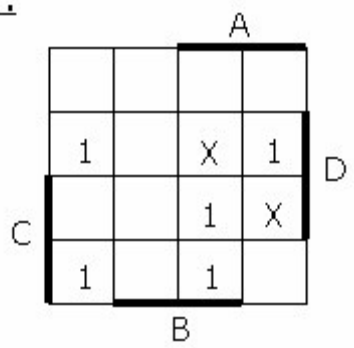
Your solutions are due on Friday, May 4 at the beginning of class.

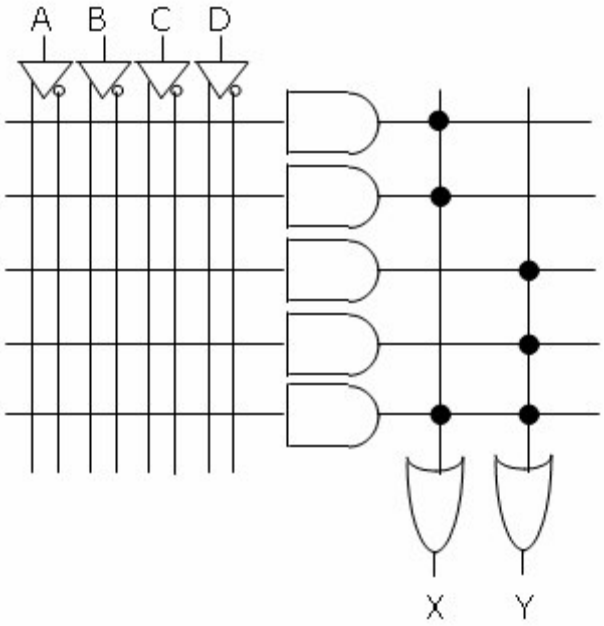
1. (20 points) Implement the functions X and Y as specified in the K-maps in the PAL provided below. Note that the PAL requires that the two functions share one product term. Label the product terms.

X:



Y:





2. (20 points) Identify and correct all the errors in the following Verilog code:
(4 points for each error correctly identified; -2 points for each mis-identified)

```
 1  // A and B are inputs.  The outputs eq, gt and lt are 0 by default.
 2  // If A = B, eq is 1; if A > B, gt is 1; if A < B, lt is 1.
 3  module compare (eq, gt, lt, A, B);
 4    input A, B;
 5    output eq, gt, lt;
 6    wire notA, notB;
 7    wire C, D;
 8
 9    not n1(A, notA);
10    not n2(B, notB);
11    and a1(C, A, B);
12    and a2(D, notA, notB);
13    or  o1(eq, C, D);
14
15    assign gt = A & notB;
16
17    always @ (B or notA)
18    begin
19      lt = B & notA;
20    end
21  endmodule
22
23  // Same concept, but this time compare 2 bit numbers
24  module compare2 (eq, gt, lt, A, B);
25    input [1:0] A, B;
26    reg [1:0] eq2, gt2, lt2;
27    wire C;
28    reg D, lt;
29
30    compare c1(eq2[0], gt2[0], lt2[0], A[0], B[0]);
31    compare c2(eq2[1], gt2[1], lt2[1], A[1], B[1]);
32
33    assign eq = &eq2;
34
35    or  o1(gt, gt2[1], C);
36    and a1(C, eq2[1], gt2[0]);
37
38    always @ (lt2[1] or eq2[1])
39    begin
40      lt = D | lt2[1];
41      D = eq2[1] & lt2[0];
42    end
43  endmodule
```

Sample Answer:

```
   1)  Need to declare lt as "reg" in compare
```

(now find 5 more errors, 4 points each)

—OVER—