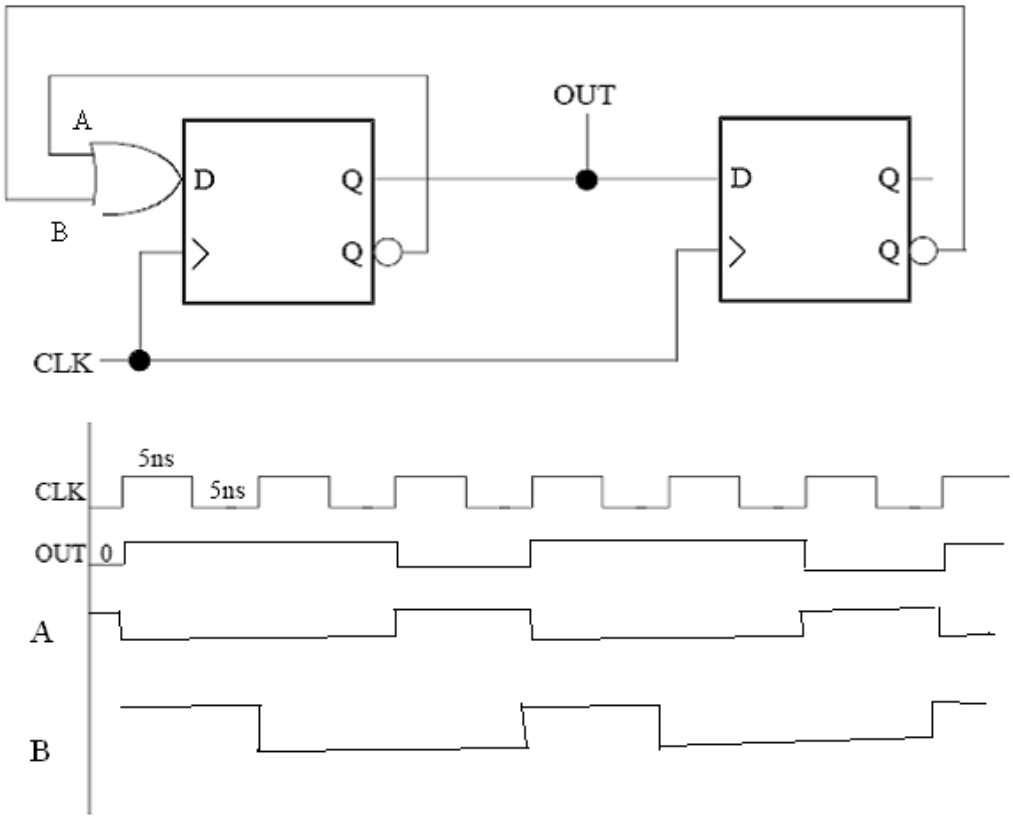
Name:

CS370: Introduction to Digital Design — Instructor: B. Hemingway

Exam #2

Nov 23, 2009

1. You are given the following circuit:



(a) (20 pts) Assuming a clock input as shown, and that OUT=(logic 0) at time t=0ns, draw a timing diagram. Label and draw OUT's timing, and also show the timing for any internal nodes that you use to derive OUT.

(b) (15 pts) **What is OUT's duty cycle?** _____2/3 or 66%_____

(c) (20 pts) The clock frequency is 100MHz. Indicate by checking either (y) or (n) whether flip-flops with the following propagation delays, setup times, and hold times will work satisfactorily in this circuit. Assume that the OR gate has zero propagation delay.

(y) (n)	Propagation delay	Setup time	Hold time
( ) (x)	10ns	10ns	10ns
( ) (x)	5ns	5ns	6ns
( ) (x)	6ns	2ns	6ns
(x) ( )	6ns	3ns	3ns

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2. 5 pts.

(F)T/F? Applying S=0 and R=0 to an S-R latch is an invalid input, because the output can enter a race condition.

(F)T/F? A flip-flop's propagation delay, from a change in the clock edge to a change in the output, typically is shorter than the flip-flop's hold time, so you can construct shift registers from cascaded flip-flops.

(F)T/F? **A** Moore state machine usually has fewer states than the equivalent Mealy machine.

(F)T/F? A D flip-flop samples its input on one edge of the clock, and changes its output on the other edge.

3. (25 pts)