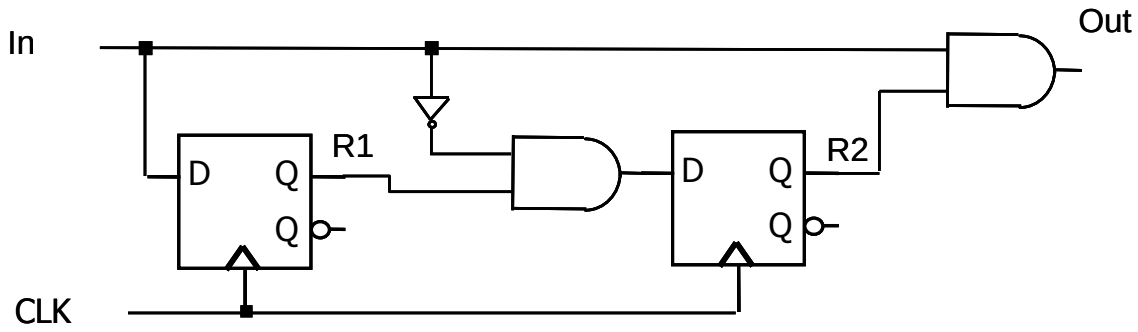
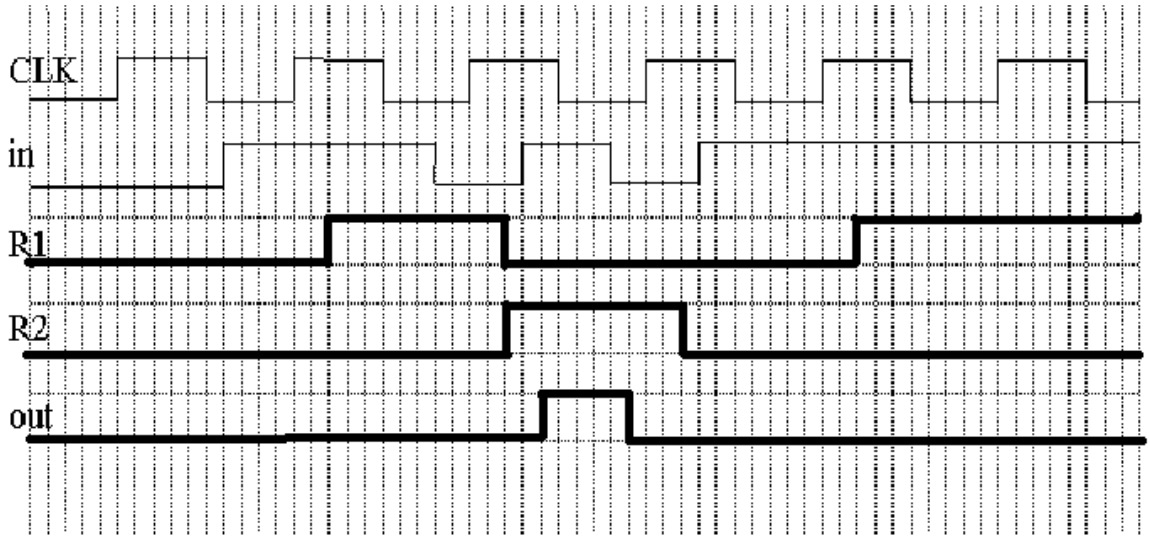
CSE 370 Midterm 2

Winter 2009

Problem 1: (20 points)

Fill out the timing diagram for the following circuit. The clock period is 10 ns as marked on the diagram. Assume that each D flip-flop has a propagation delay of 2 ns and hold time of 1 ns. Assume that each gate (inverter or AND) has a gate-delay of 1 ns. As shown on the timing diagram, assume that all signal rise and fall times are instantaneous.





The original question had no set-up time listed which I corrected in class to 1 ns set-up time. Unfortunately, the signal into the second flip-flop did not respect this set-up time and transitions to high exactly on the 3rd positive clock edge. This means that it was also correct to have this signal ignored by the second flip-flop which would leave both R2 and out low throughout the time period. Such solutions also received full points.

Problem 2: (10 points)

Which of the following must always be true for proper operation of a sequence of identical flip-flops (circle the correct answers):

(2 pts) (a) The set-up time cannot exceed the clock width?

F There is no connection between the two. Clock width is not clock period

(2 pts) (b) The hold time must be less than propagation delay?

T This is one of the two essential requirements.

(2 pts) (c) The clock period must be larger than the propagation delay plus the hold time?

F Hold time and propagation delay overlap in time

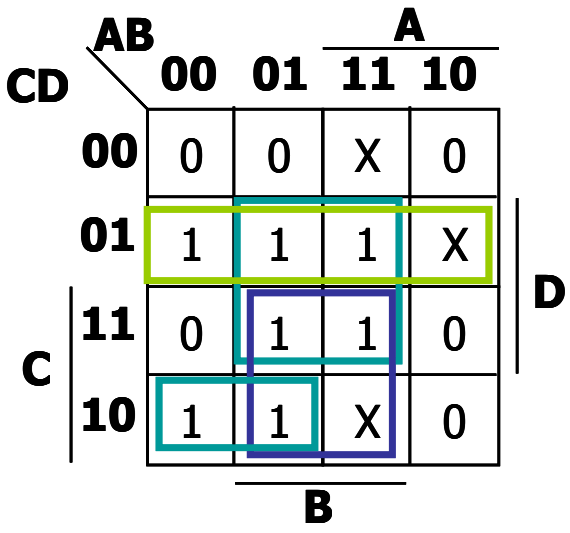
(2 pts) (d) The clock width must be larger than the propagation delay?

F These overlap but there is no need that one be longer than the other

(2 pits) (e) The set-up time plus the propagation delay must be less than the clock period?

T Propagation delay and set-up time cannot overlap

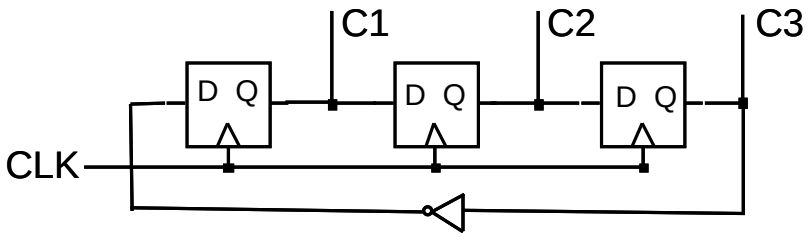
Problem 3: (10 points)
Given the following K-map for a function F, design a minimized sum-of-products for F that avoids static-1 hazards.

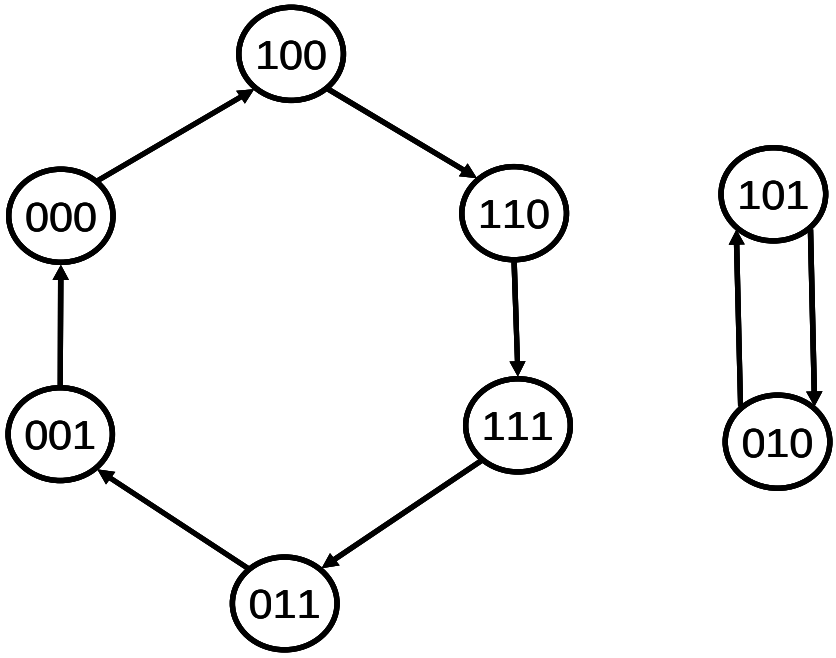


F=BC+BD+C'D+A'CD'

Problem 4: (20 points)

(a) (12 points) Draw the complete state diagram for the following counter:





(b) (3 points) This counter is not self-starting. Why not?

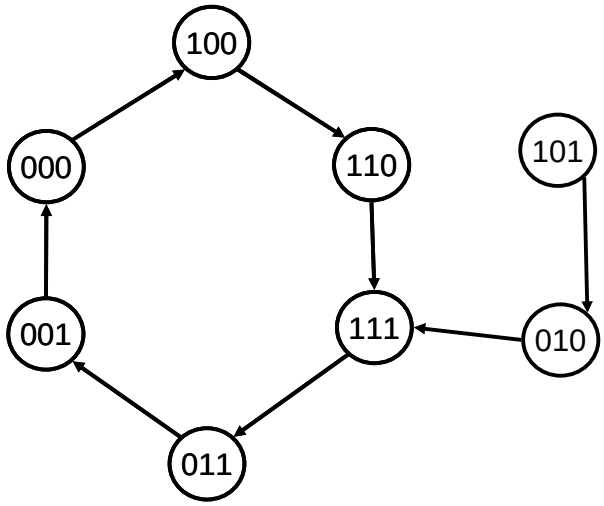
There are two separate loops. If counter is started in states 101 or 010 it will loop forever without reaching one of the other 6 states (and vice versa).

(c) (5 points) How specifically would you change the state diagram to make this counter self-starting?

Change the transition out of state 010 to point to state 111 and leave the rest the same so that no matter where the machine starts it will end up in the 6 state loop. See the revised state diagram on the following page. (Many other options are possible.)

(d) (5 points extra credit) Show how to modify the circuit for this counter so that it will have the same functionality started from 000 but will implement your design change from part (c). Be sure to minimize your design.

We will implement a circuit for the state diagram on the right. There are 47 other designs that would work.



The transition table is the following:

C1	C2	C3	$C1^+$	$C2^+$	$C3^+$
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	1	1	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	1
1	1	1	0	1	1

$C1^+$

C3 \ C1C2	00	01	11	10
0	1	1	1	1
1	0	0	0	0

C1 (over 11, 10) C2 (under 00, 01)

$C2^+$

C3 \ C1C2	00	01	11	10
0	0	1	1	1
1	0	0	1	1

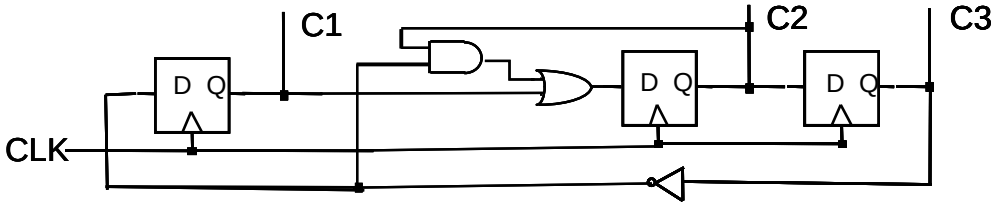
C1 (over 11, 10) C2 (under 00, 01)

$C3^+$

C3 \ C1C2	00	01	11	10
0	0	1	1	0
1	0	1	1	0

C1 (over 11, 10) C2 (under 00, 01)

$C1^+ = C3'$
$C2^+ = C1 + C2\,C3'$
$C3^+ = C2$

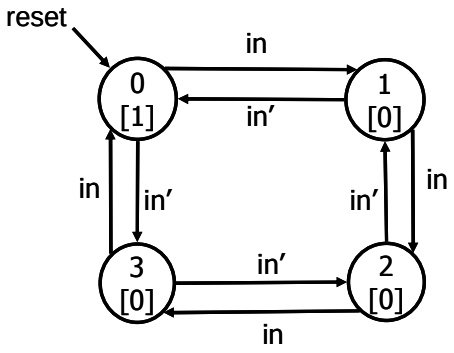


Problem 5: (40 points)
In this problem you will build a 4-state cyclic counter with an additional single binary input. When the input is 1, the counter should increment by one; when it is 0, the counter should decrement by 1. There is also a separate Reset signal that returns the counter to value 0. To encode the states of your counter use the Gray Code encoding in which 0 is encoded as 00, 1 is encoded as 01, 2 is encoded as 11, and 3 is encoded as 10. (This will make your design simpler.) Your counter also should have a single output bit that is 1 if and only if the current value of your counter is 0; i.e., the difference between the number of 1's and 0's input since the last Reset signal is divisible by 4.

Show the following 4 steps:

(i) Draw a state diagram of your counter and minimize it.
(ii) Fill in a state transition table using the above encoding
(iii) Minimize your logic using K-maps
(iv) Implement your design as a circuit using D flip-flops having a separate Reset input.

Input bit: in **(i)**



(ii) Encoding: State 0 = 00, State 1 = 01, State 2=11, State 3=10

S0	S1	in	S0+	S1+	out
0	0	0	1	0	1
0	0	1	0	1	1
0	1	0	0	0	0
0	1	1	1	1	0
1	0	0	1	1	0
1	0	1	0	0	0
1	1	0	0	1	0
1	1	1	1	0	0

(iii) Minimize Logic

$S1^+$

in \ S0S1	00	01	11	10
0	0	0	1	1
1	1	1	0	0

S1

$S0^+$

in \ S0S1	00	01	11	10
0	1	0	0	1
1	0	1	1	0

S1

$S1^+$ = in S0′ + in′ S0
= in ⊕ S0
= in xor S0

$S0^+$ = in′ S1′ + in S1
= (in ⊕ S1)′
= in xnor S1

output = S0′ S1′
= S0 nor S1

(iv) Circuit Implementation