

# CSE 370 Homework 5 Solutions

## 1. ALU Design

The design of the ALU should begin at the single bit level. For the operations specified in the problem statement, only three modifications need to be made to the 1-bit full adder in order to construct an ALU. First, the XOR, XNOR, and PASS\_A operations all require the ability to set the generate signals to 0. To do this, and the generate signal with a control bit. Next, the INCREMENT and PASS\_A operations require B to be set to 0. This requires the input B to be AND'ed with another control signal. Lastly, the XNOR and SUBTRACT operations require the ability to flip all the bits of A. This is accomplished by XOR'ing A with the final control signal. These 1-bit full adders are then implemented as 4-bit independent full adders, like was done in the 16-bit carry look-ahead adder implementation.

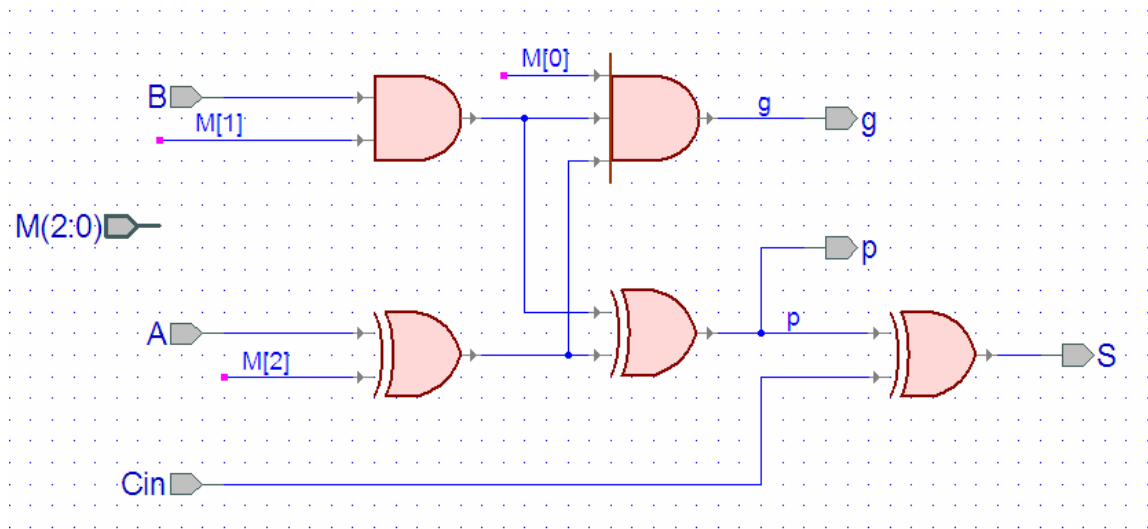


Figure 1: 1-bit adder for the 16-bit ALU.

The top level of the 16-bit ALU appears very similar to the top level of the 16-bit CLA that we designed in the previous homework. The main difference is the control signals that are routed to each of the independent full adders. Also, the top level contains the logic to generate the control signals for the full adders, based on the inputted opcode. The control signal logic is shown in Figure 3.

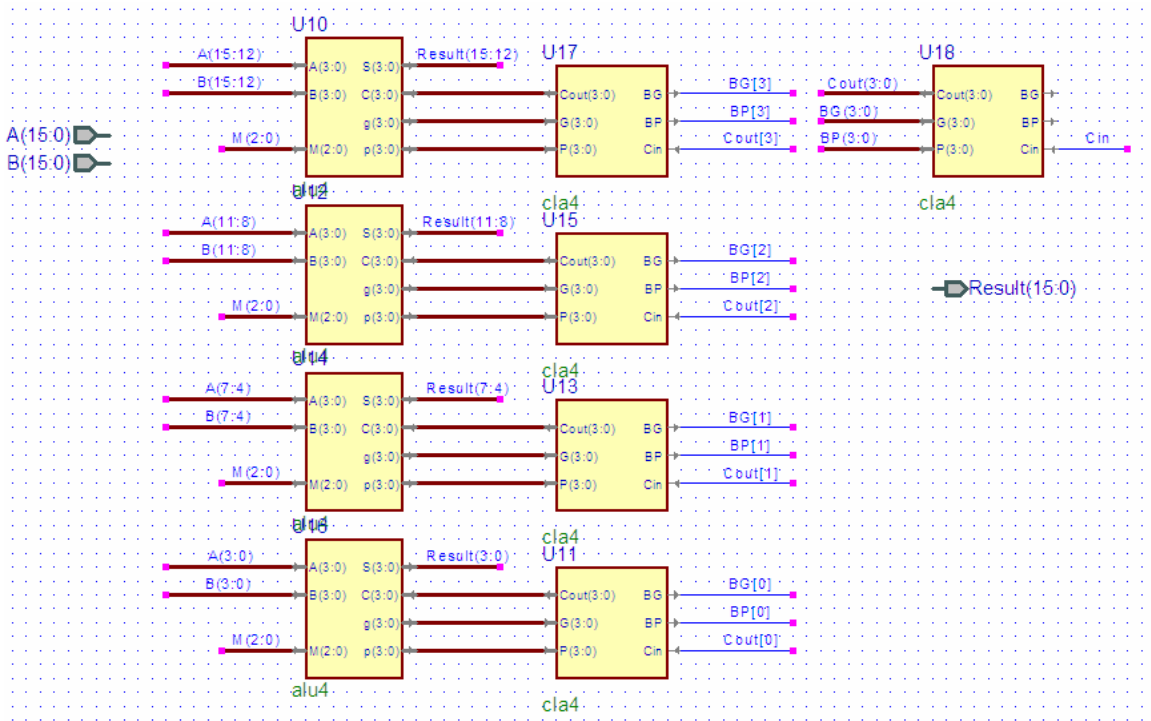


Figure 2: Top level circuit for the 16-bit CLA. Not shown here is the control signal generation circuit.

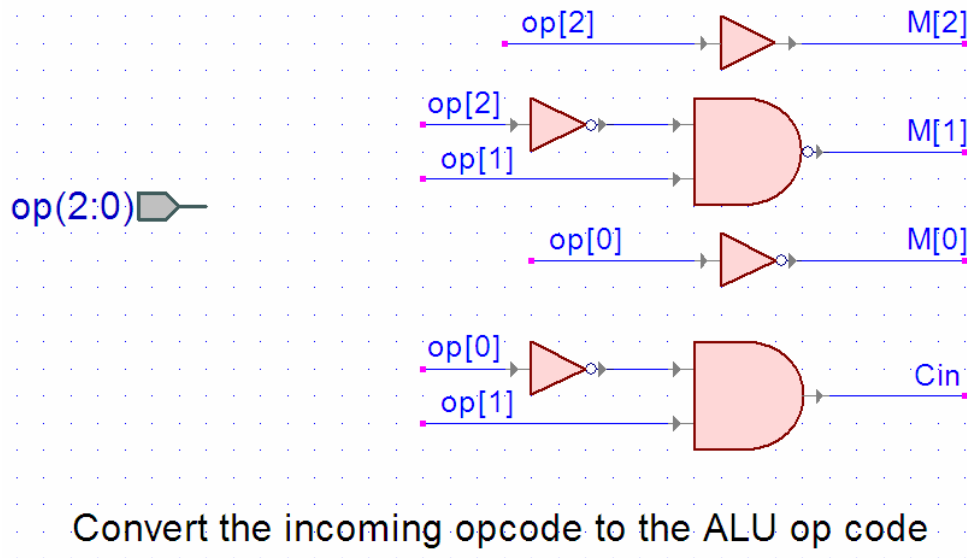


Figure 3: Logic to generate the control signals for the adders; based on the input opcode.

## 2. Sequential Circuit

This circuit detects the condition when 2 or more 1's have been seen within a window of 3 clock cycles. However, it is delayed by 5 clock cycles from the time of the first 1 being shifted in.

The following modified circuit detects 4 consecutive 1s on the input.

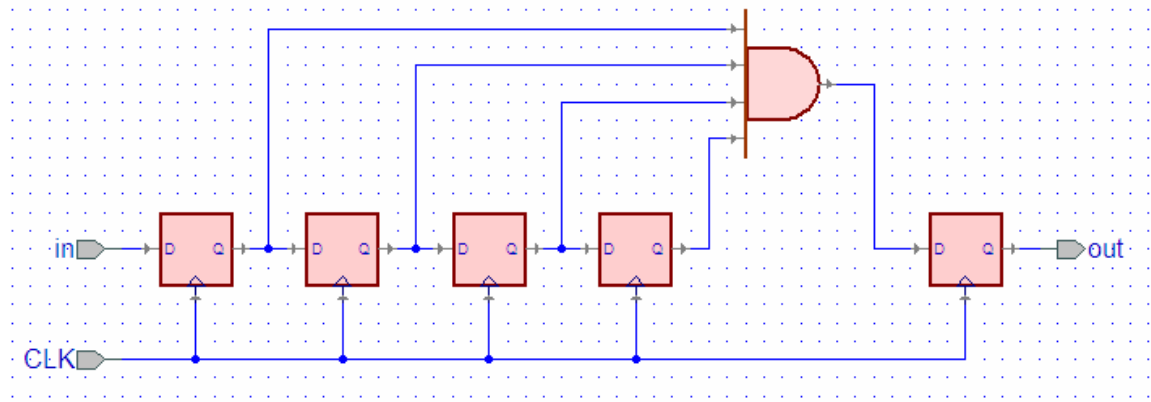


Figure 4: Circuit to detect four consecutive 1's on the input.

### 3. Sequential Timing

Gate delay = 1ns, Register delay = 2ns, time markings on diagram are 1ns steps

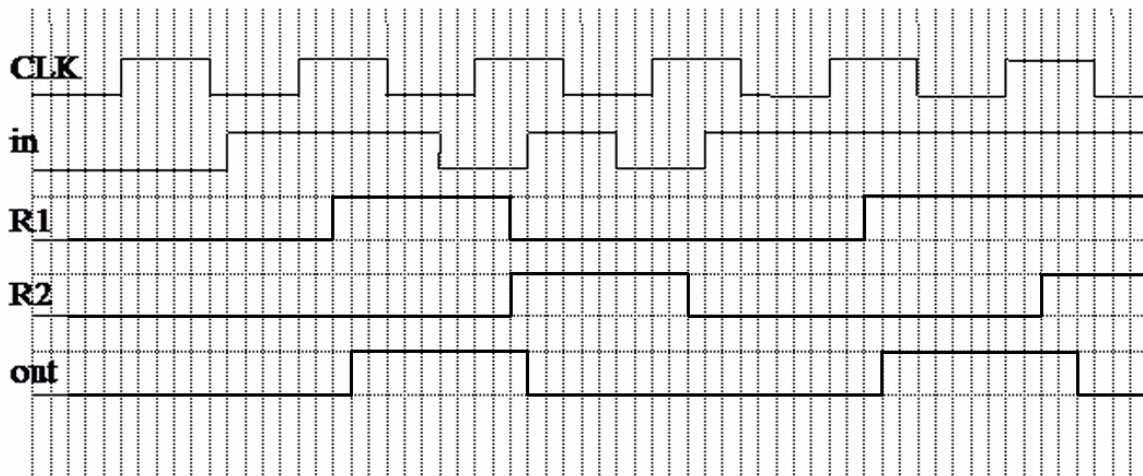


Figure 5: Timing diagram for '01' sequence detector.

- a) Shown here is the state diagram for this Moore type state machine. Note that the output is a function of the state only, so the output value is shown with the current state. For this solution, the state is shown as [R2,R1], (R1 is the least significant value).

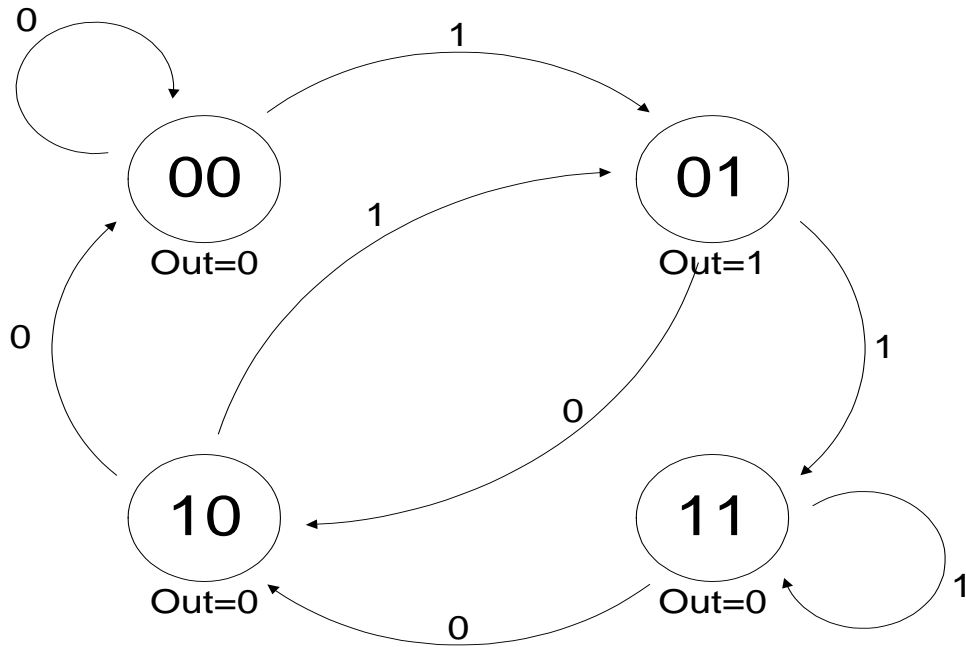


Figure 6: State diagram for the given circuit. Notice the output value is listed with the state for this Moore type state machine.

#### 4. State Diagram

Note: The circuit in Figure 7 shows that the upper flip-flop is considered the most significant state bit in the solution.

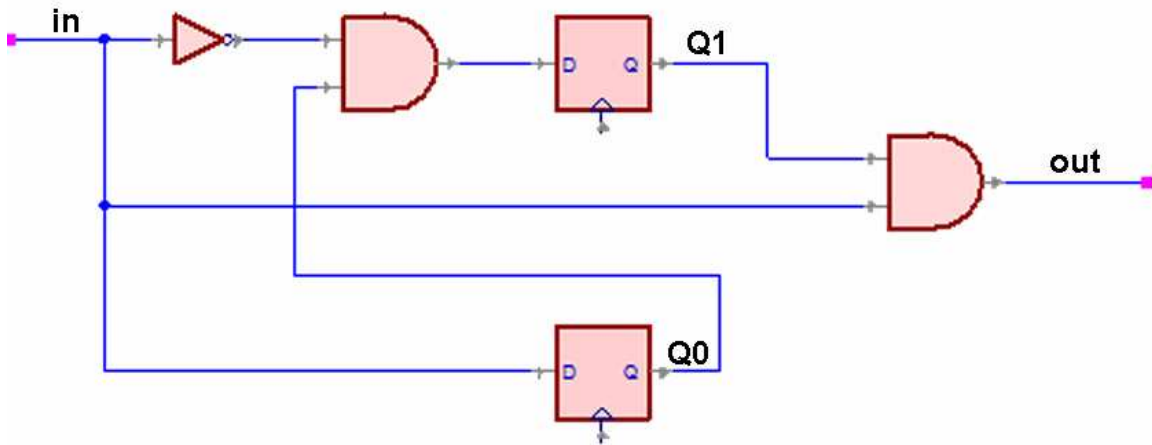
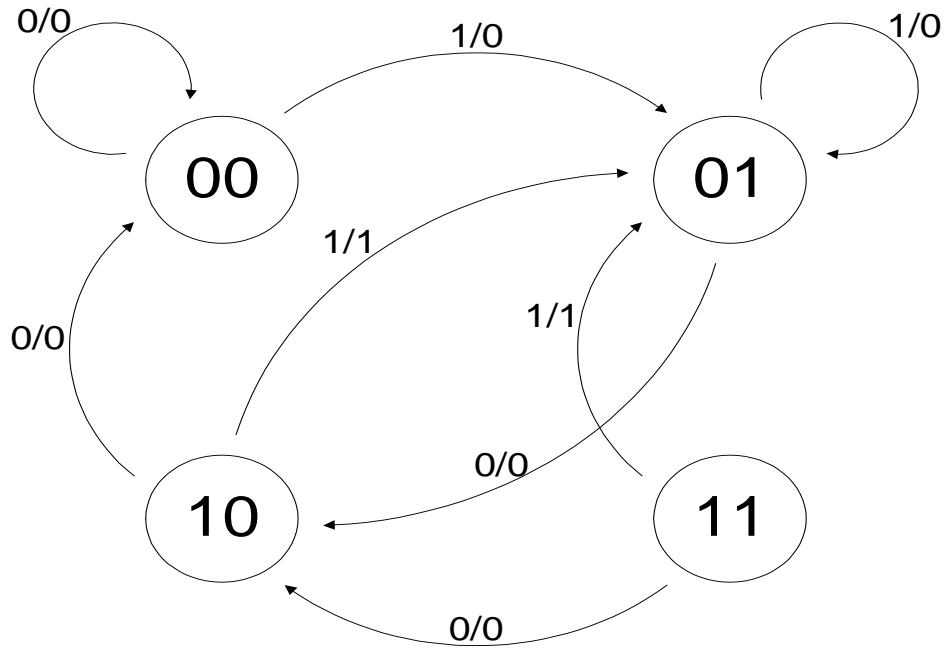


Figure 7: Circuit to draw the state diagram based on. Notice that the top flip-flop is the most significant, so state 10 represents a 1 at Q1, and a 0 at Q0.

Shown in the following figure, Figure 8, is the state diagram for the given circuit.



**Figure 8: State diagram for the specified Mealy type state machine. Notice the output is listed along the transitions with the inputs, because the output is a function of the current state and the input.**