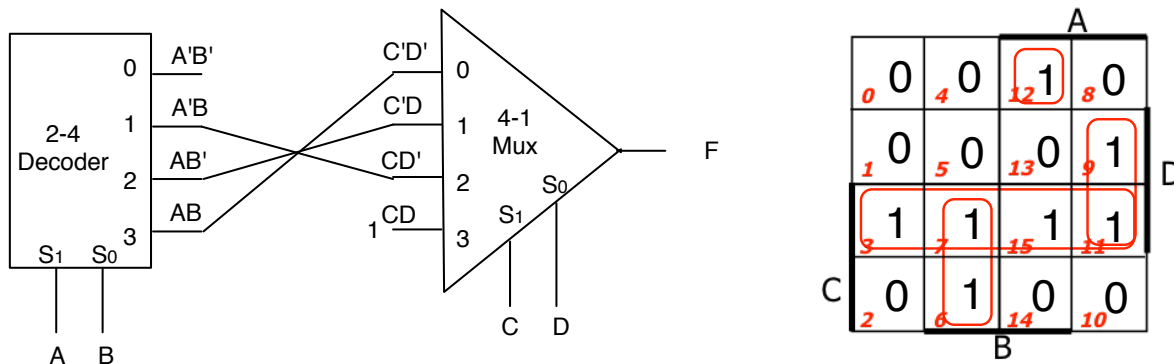


**CSE 370 - Introduction to Digital Logic Design
Spring 2010
Quiz #4 - Solution**

For maximum credit, show all your work. Please raise your hand if you have a question.

1. Write down the Boolean function computed by the following circuit. Any representation is fine. (The wires do not touch where they cross.)

$F = A'BCD' + AB'C'D + ABC'D' + CD$



2. How many AND gates are used in total to implement this circuit? That is, how many AND gates are there in all in the decoder and multiplexer? No credit for just writing a number for parts 2, 3, & 4 – you must explain how you got it.

8 – 4 for the decoder (1 per output) and 4 for the multiplexer (1 per input)

3. How many AND gates would there be in the smallest ROM that implements this function?

16 – You need a ROM with 4 inputs which automatically computes all 16 minterms with 16 AND gates.

4. What is the smallest number of AND gates needed by a PLA implementation of this circuit?

4 – See the K-map for the minimized function.