

CSE 370 – Introduction to Digital Logic Design
Spring 2010
Quiz #7

For maximum credit, show all your work. Please raise your hand if you have a question.

Draw a circuit that implements the following Verilog module description. Use only simple registers, with only clock, D and Q.

```

module what
  (input clk,
   input A,
   input B,
   input [1:0] C,
   output [1:0] D);

  reg [1:0] X, Y;
  assign D = B ? Y : X;
  always @(posedge clk)
    if (A)
      if (B) X <= C;
      else Y <= C;
endmodule
  
```

Note that this problem is almost like the register file except that there are only two registers. A is the Write control signal and B is the Read and Write address (but used in reverse order).

