CSE 370 Fall 99
Solution for Assignment 2
10/12/99

1.a)

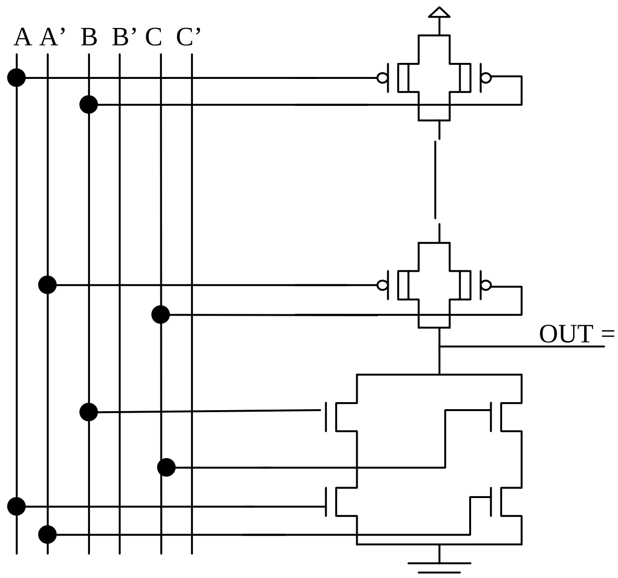
Reading the pMOS (top) part directly

F = (A’+B’)(B’+C’)(A+C’)

Also to recheck you should read the nMOS part directly

F’=AB+BC+A’C

And check that these expressions are negation of each other.



(F’)’= (AB+BC+A’C)’=(AB)’(BC)’(A’C)’
= (A’+B’)(B’+C’)(A+C’)
(DeMorgans Law all the way!)

b)

Applying the consensus Theorem on F’ results in following simplification on F’

F’= AB + A’C

A more elaborate proof

F’ = AB+A’C+BC
=AB+A’C+BC(A+A’)
= AB+ABC+A’C+A’BC
= AB(1+C)+A’C(1+B)
= AB+A’C

c)

part a) : 12 transistors
part b): 8 transistors
so four transistors saved .Hence 8μm^2 area saved.

1. a)

To prove that NAND is complete show that NOT,AND & OR gates can be implemented using the NAND gates.

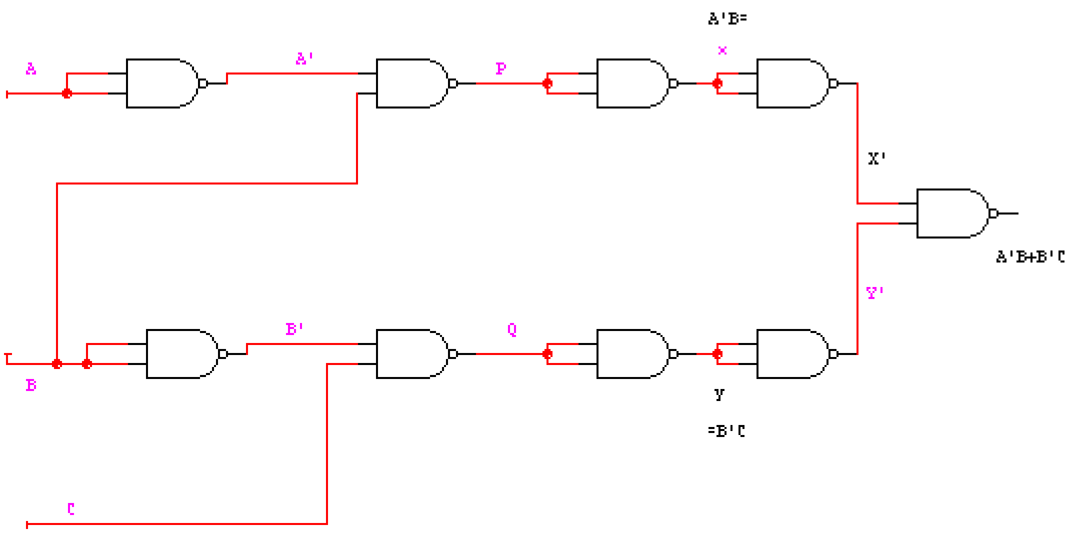
A’ = (A + A)’ = A nand A
AB = ((AB)’)’ = (A nand B)’ = ((A nand B) nand (A nand B))
A+B = ((A+B)’)’ = (A’ B’)’ = (A’ nand B’) = ((A nand A) nand (B nand B))

b)

F=A’B+B’C

= (A nand A)B+(B nand B)C (using the not expansion)
= X + Y (Let)
so using the expansion for AND gate interms of nand
X = (A nand A)B = [(A nand A)nand B)] nand [(A nand A)nand B)]
Y = (B nand B)C = [(B nand B) nand C)] nand [(B nand B) nand C)]

And
F=X+Y = (X nand X) nand (Y nand Y)
So we get the following schematic.



The opportunity for minimization is evident by the diagram. Note that from P to X' there are two NOT gates (implemented using NAND) . So they are redundant and hence can be removed. Same for Q and Y'. So the inputs P and Q can *directly* be used as inputs for the final (rightmost) NAND gate.

5.

a) The truth table for function P is shown below.

A	B	C	P(A,B,C)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Reading directly form the truth table:
$P(A,B,C) = A'B'C + A'BC'+AB'C'+ABC$

b) XOR can considered as a two-input parity function . So obv.
$P(A,B,C) = (A \text{ xor } B) \text{ xor } C$
More formally, proof goes as follows

First of all note that
$A \text{ xor } B = A'B+AB'$
And hence
$(A \text{ xor } B)' = A'B' + AB$

Now for the proof
$P(A,B,C)=A'B'C+A'BC'+AB'C'+ABC$
$= C(A'B'+ AB) + C'(A'B+AB')$
$= C(A \text{ xor } B)' + C'(A \text{ xor } B)$
$= C \text{ xor } (A \text{ xor } B).$

c)
The function P (the wire P) is 1 when three are odd number of 1's in A,B and C. This implies that together P,A,B and C should **always** have even number of 1's if transmitted correctly i.e. They should always have their parity as 0 in case there is no error.

A	B	C	P	E(A,B,C,P)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

d) Using the same intuitive argument as above we get
$E(A,B,C,P)= (A \text{ xor } B) \text{ xor } (C \text{ xor } D)$

A more formal proof would be on same lines as in part b) above basically grouping

Terms with C’D’, C’D, CD’, CD together first then basis of D and D’ and finally as a whole one big term. The schematic is drawn below
NOTE: XOR is associative.