CSE370 Fall '99
Assignment 3
Distributed: 10/11/99
Due: 10/18/99

Reading:

Katz, Chapter 2 (pp. 40-83) same as last week!

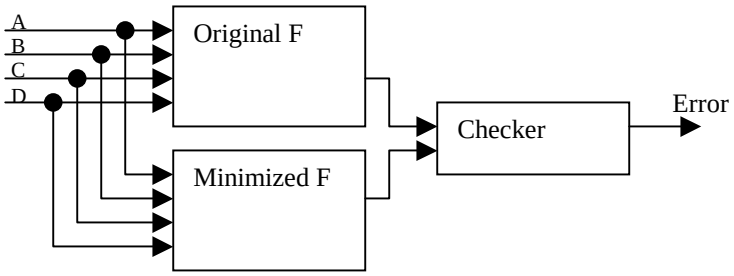
Exercises:

1. **Do parts *b* and *c* below. Part *a* was due last week and will not be regraded. (4pts)**

   a) **Included for reference only** Using only AND-OR-NOT logic, create a schematic in DesignWorks (DW) that directly implements the following function: **F(A,B,C,D) = (AD+A'C)[B'(C+BD')]**. In DW, do the following:
   - Set the delay for each gate to 10 time units. See *courses/370/98au/admin/Tools/DesignWorks/Tips.html* for tips on how to set gate delay. Tip number 6 on this web page is useful for setting any delay, not just zero.
   - Create a complete set of input test stimuli for your circuit using the DW Test Vectors spreadsheet tool (refer to DW webpage under "Generating useful output"). Your input vectors should change every 80 time units.
   - Simulate your test vectors and turn in the schematic and timing diagram (waveforms) showing **ABCD** and **F**. Save your design for the next step.

   b) Using Boolean algebra, find a minimized **two level** expression for the function of Assignment 2 part *a*, and enter the circuit into DW. Repeat the steps above for this implementation of **F**.

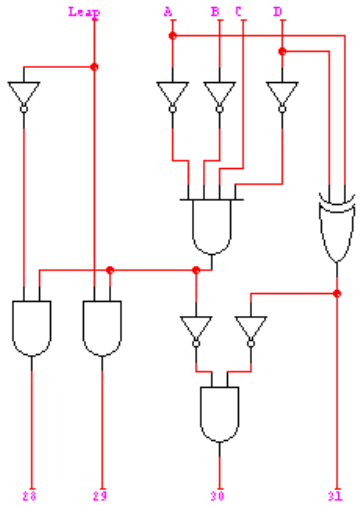
   c) Verify that the original and minimized circuits are equivalent using the "expected output" feature of the DesignWorks test vector spreadsheet tool. One way to do this is to enter into the spreadsheet the expected output for every input. However, that would be a lot of work for a very large design. It might be easier to design a third combinational circuit, called **CHECKER**, that simply compares the output of the two designs and generates an error signal if they are different, as shown in the figure above. The expected value for **Error** should always be "0". Using CHECKER, you should be able to verify your optimized design without even knowing the expected output for all inputs.



   Turn in the flat (not hierarchical) gate level schematic for the entire circuit shown in the figure along with a printout of the test vector spreadsheet from DesignWorks showing that the two implementations of **F** are equivalent. Also, turn in the timing diagram for the simulation. **Is *Error* always zero in the timing diagram? Explain**. Note: you can build the verification schematic by cutting and pasting the original design into the same schematic page with new design.

2. **Verification using Boolean Algebra (4pts)**

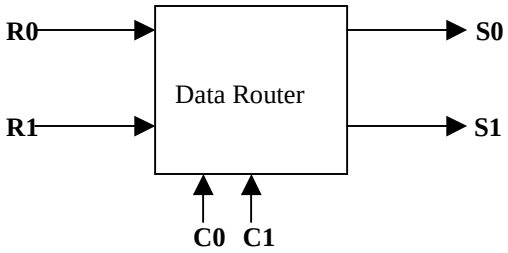
a) Find a canonical form for each of the calendar system outputs that were defined in lecture. Please use the same month encoding that was used in class. That is (Jan = 1, Feb = 2,…, Dec = 12). Note that in lecture we used **(m1, m2, m3, m4)** as names for the month inputs to the circuit. Please do not confuse these signal names with minterm identifiers. To avoid confusion, please use (leap,a,b,c,d) as the input signal names and ordering for your canonical expressions. Please use the "little m" and "big M" shorthand notations for canonical forms described in Katz and in lecture. For example, you should write **28(leap,a,b,c,d) = …**



b) Using Boolean algebra, verify that the circuit design for the calendar system shown at right (from lecture) is correct for each output **(28,29,30,31).** Your proof should show that each of the outputs is equivalent to one of its canonical forms.

3. **Telecom Switch Design (4 pts)**

Please design a 2x2 switch for use in a data router. The device receives data on inputs **R0** and **R1**, and sends data out on **S0** and **S1**. The device can perform four different routing functions shown in the table below. The function determined by the inputs **C0** and **C1**.



Control Inputs C0 C1	Function	Definition
0 0	Broadcast **R0**	Send **R0** out on both **S0** and **S1**
0 1	Broadcast **R1**	Send **R1** out on both **S0** and **S1**
1 0	Pass Through	Send **R0** out on **S0** and send **R1** out on **S1**
1 1	Exchange	Send **R0** out on **S1** and send **R1** out on **S0**

a) Construct a truth table showing the inputs and outputs of the system and write the canonical SoP and PoS expressions for **S0(R0,R1,C0,C1)** and **S1(R0,R1,C0,C1)** using minterm and maxterm notation.

b) Using Boolean algebra, minimize the functions for **S0** and **S1.**

4. **Boolean Simplification (4pts)**

Problem 2.13 in Katz

5. **Canonical Forms (4 pts)**

Problem 2.15 in Katz