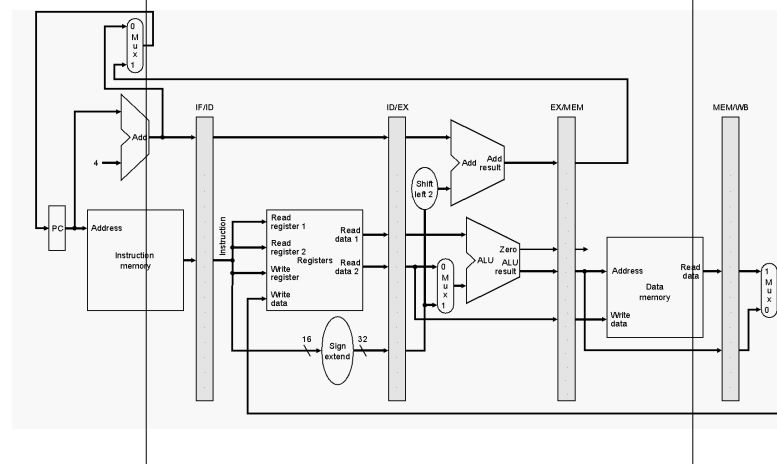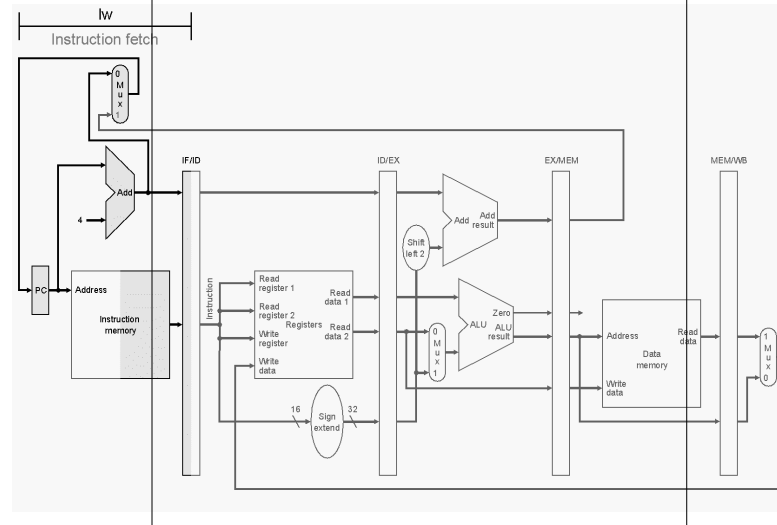# Operation of a Pipeline

Each stage of a pipeline must be controlled
independently of the other stages … pipeline registers
make this happen
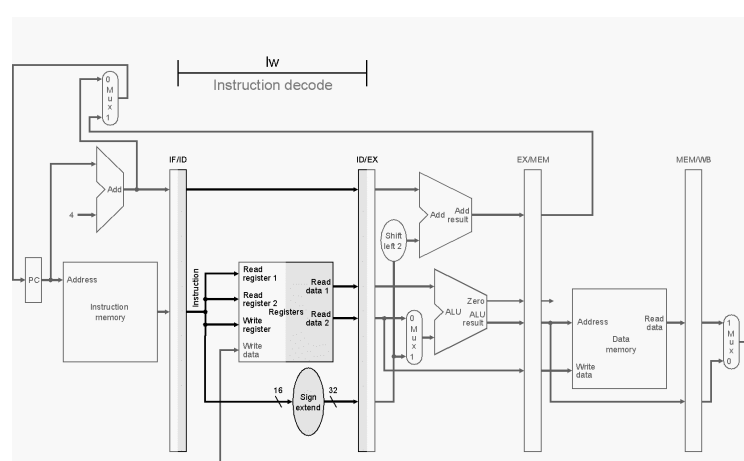
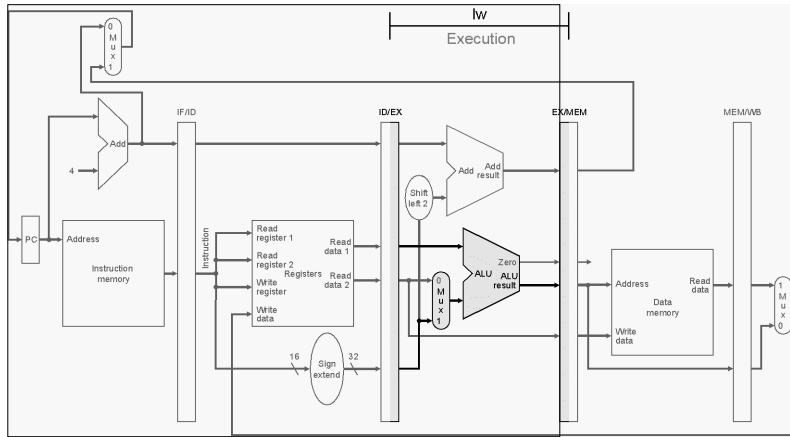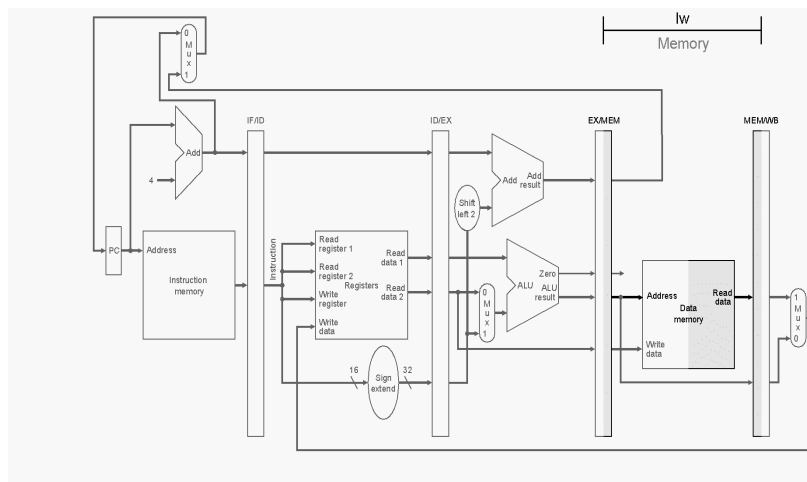# Pipeline Registers

Stage 1, LW

lw

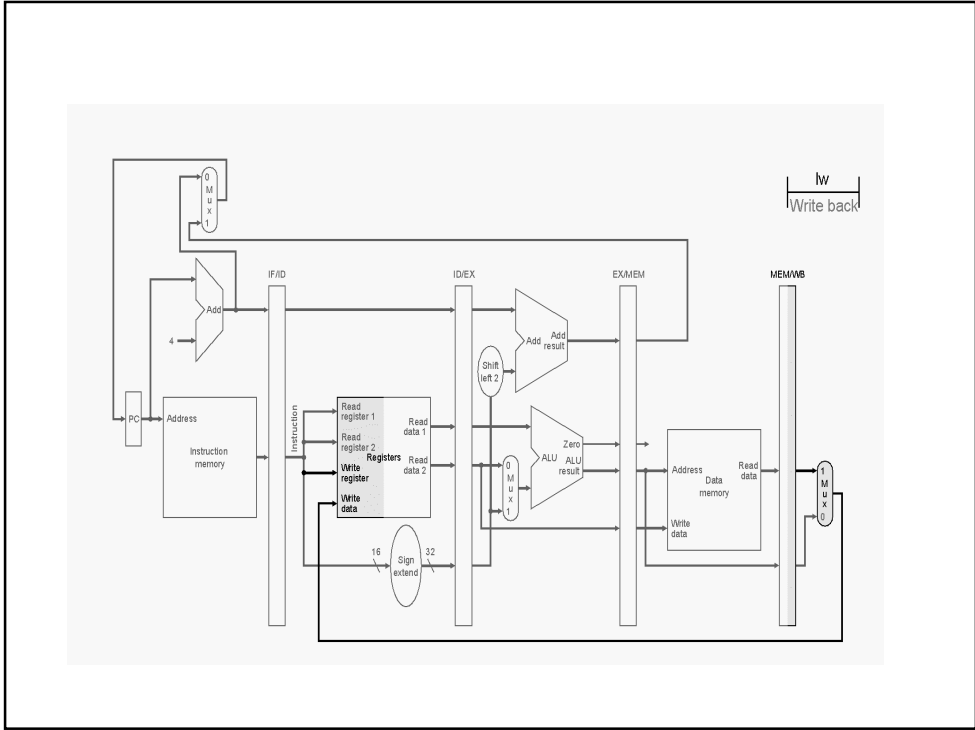Instruction fetch

Stage 2, LW

lw

Instruction decode

Stage 3, LW

Stage 4, LW

0
Mux
1

IF/ID   ID/EX   EX/MEM   MEM/WB

Add

4

Add
result

Shift
left 2

PC   Address

Instruction
memory

Instruction

Read
register 1

Read
register 2

Registers

Write
register

Write
data

Read
data 1

Read
data 2

0
Mux
1

Zero
ALU
ALU
result

Address

Data
memory

Write
data

Read
data

1
Mux
0

16   Sign
extend   32

LW Write Back

0
Mux
1

IF/ID   ID/EX   EX/MEM   MEM/WB

Add

4

Add
result

Shift
left 2

PC   Address

Instruction
memory

Instruction

Read
register 1

Read
register 2

Registers

Write
register

Write
data

Read
data 1

Read
data 2

0
Mux
1

Zero
ALU
ALU
result

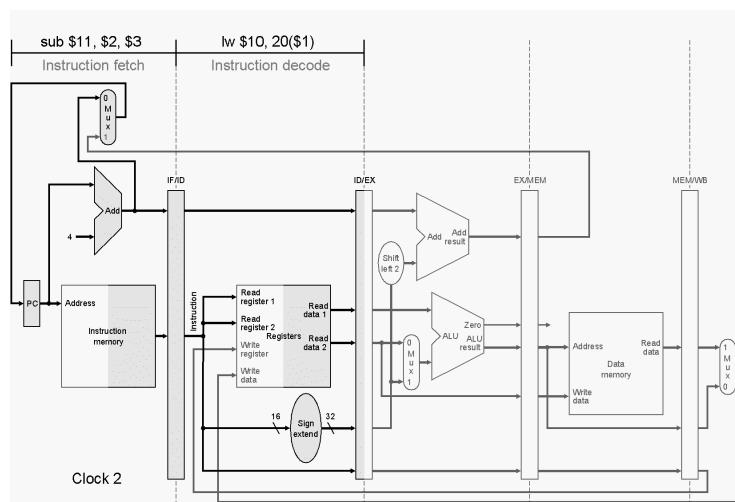Address

Data
memory

Write
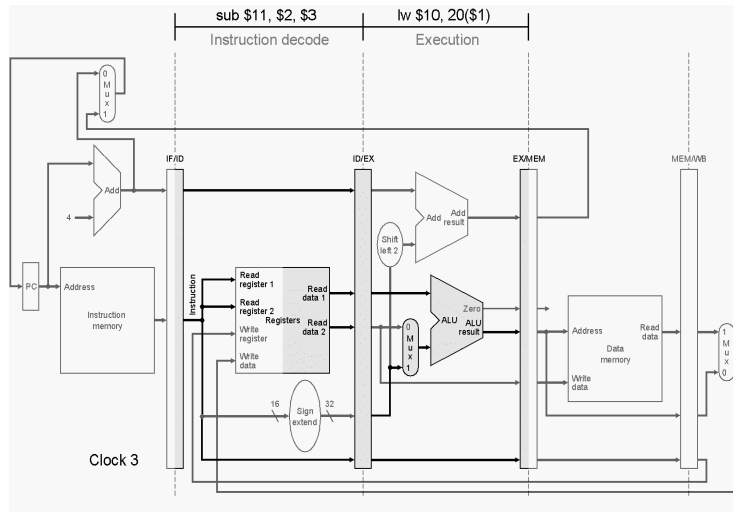data

Read
data

1
Mux
0

16   Sign
extend   32

Stage 4, SW

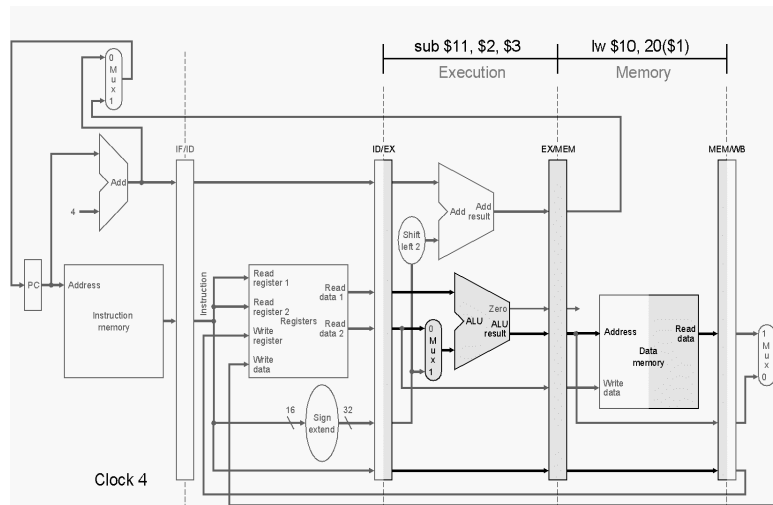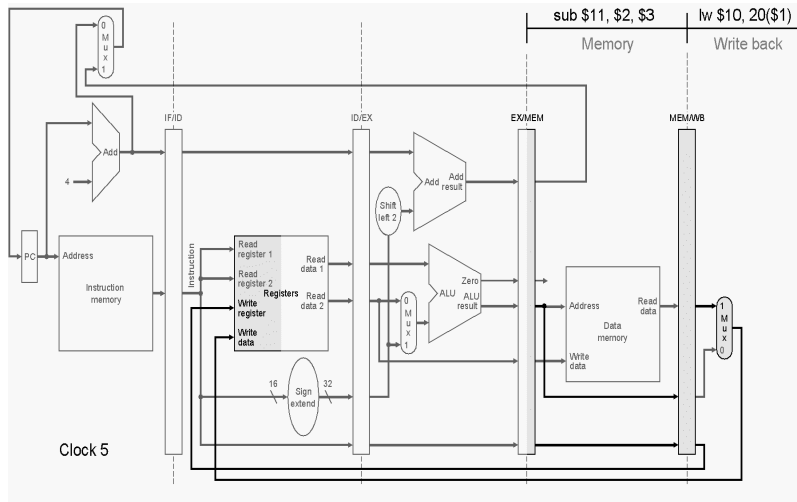# Two Instructions In Pipe

Advance Instructions: 2,3

Advance Clock: 3,4

Advance Clock: 4,5

sub $11, $2, $3   lw $10, 20($1)

Memory   Write back

Clock 5

Advance Clock: 5

sub $11, $2, $3

Write back

Clock 6