Midterm Topics

The midterm (which is closed everything) will cover course material up through sections yesterday, PLUS a basic understanding of forwarding as a way to handle data hazards in pipelined implementations.

Questions will assume you've attended lectures and sections, done the reading in the text, done the reading of other handouts, looked at sample code available from the course calendar, done the assignments, looked at sample assignment solutions.

Performance

- Measures of performance (both time and power)
- Relative speedup
- Amdhal's Law
- Moore's Law
  - The motivation for multicore architectures

Single Cycle Datapath

- Components and connections (i.e., the datapath)
- Execution of instruction types
- Implementation of control

Multi-cycle Datapath

- When/why is it faster than single cycle?
- "Pipeline registers": why we need them / what they're for
- Basic idea of the implementation of control

Pipelined Datapath

- When/why is it faster than single cycle?
- How is the MIPS ISA "designed for pipelining"?
- Why isn't the pipelined datapath in the book five times faster than the single cycle datapath in the book?
- Dependences: Read-after-write, write-after-read, write-after-write (read-after-read)
- Data hazards:
  - compiler inserts nop's
  - control inserts bubbles
  - basic idea of forwarding

Supporting an OS

- Address translation
- Memory mapping
- Exception handling (including going back to user mode from privileged mode execution (rfe))
- Drivers and IO library functionality
- boot process

IO

- basic operation
  - communicating with controllers
- DMA vs. polling
- busy waiting vs. interrupt driven

Assembly Language Programming Concepts

- two's complement representation of integers
- shifting and its relationship to integers
- and masks (selecting bits) / or masks (forcing bits on)
- *there won't be a big assembler program to write on this exam, but there could be some small question(s) about these topics*