# CS378: Machine Organization and Assembly Language

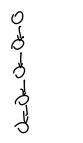
Lecture 2 – Winter 2009







What is an instruction? And a register? What does register-to-register mean? In what order is a program executed?



Why do we need memory?

Where are the instructions stored?

What is the C equivalent to: sub \$t0, \$t1, \$t2?

#### **Announcements**

- Website is up! Explore it (MIPS resources, Easter-eggs, etc)
- Homework 0 will be posted today not graded, just for your benefit
  - on your own, explore SPIM.
- Homework 1 (for a grade, to be done individually) will be posted Friday
  - write a function in MIPS assembly
  - due a week later
- Lab 1 (to be done in partners) posted next week
  - Please find a lab partner soon
  - Or we will find one for you ©
- Luis' office hours:

M 1:30-2:30, or by appointment (in CSE 576)

 Textbook – sorry about the confusion. The bookstore only sells the newest edition. Take your pick, we will post readings for both editions of the book. Check for bugs on the 4<sup>th</sup> edition.

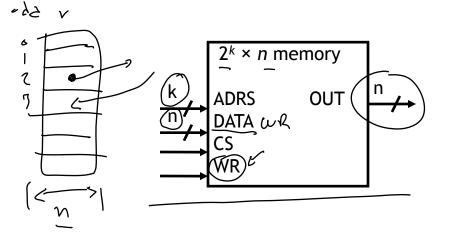
## A more complete assembly example

How would you write code in MIPS assembly to compute:

#### Memory review

l [

Memory sizes are specified much like register files; here is a RAM.

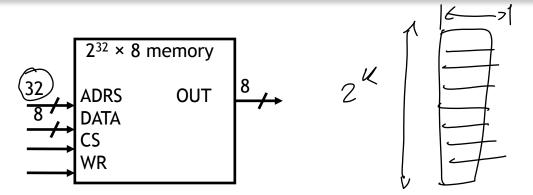


CS	WR	Operation
0	X	None
1	0	Read selected address Write selected address
1	1	Write selected address

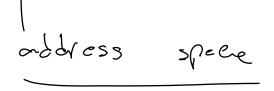
- A chip select input CS enables or "disables" the RAM.
- ADRS specifies the memory location to access.
- WR selects between reading from or writing to the memory.
  - To read from memory, WR should be set to 0. OUT will be the n-bit value stored at ADRS.
  - To write to memory, we set WR = 1. DATA is the n-bit value to store in memory.

# MIPS memory

86,7,

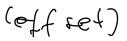


- MIPS memory is byte-addressable, which means that each memory address references an 8-bit quantity.
- The MIPS architecture can support up to 32 address lines.
  - This results in  $a(2^{32}) \times 8$  RAM, which would be 4 GB of memory.
  - Not all actual MIP\$ machines will have this much!



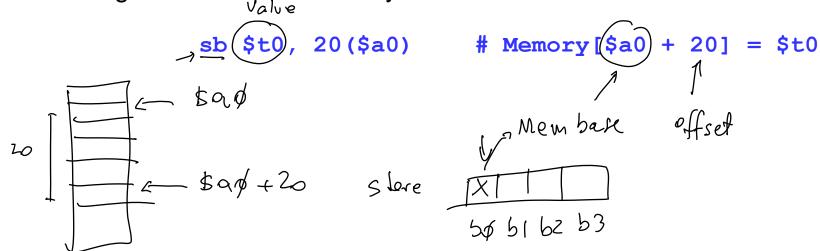
# Loading and storing bytes

- The MIPS instruction set includes dedicated load and store instructions for accessing memory
- The main difference is that MIPS uses indexed addressing.



- The address operand specifies a signed constant and a register.
- These values are added to generate the effective address.

The "store byte" instruction sb transfers the lowest byte of data from a register into main memory.



# Loading and storing words

You can also load or store 32-bit quantities—a complete word instead of just a byte—with the lw and sw instructions. ∮€ / √ | √(4) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2) | √(2)

```
lw $t0, 20($a0)  # $t0 = Memory[$a0 + 20]
sw $t0, 20($a0)  # Memory[$a0 + 20] = $t0
```

- Most programming languages support several 32-bit data types.
  - Integers
  - Single-precision floating-point numbers
  - Memory addresses, or pointers
- Unless otherwise stated, we'll assume words are the basic unit of data.

## Computing with memory

- So, to compute with memory-based data, you must:
  - 1. Load the data from memory to the register file.
  - 2. Do the computation, leaving the result in a register.
  - 3. Store that value back to memory if needed.
- For example, let's say that you wanted to do the same addition, but the values were in memory. How can we do the following using MIPS assembly language? (A's address is in \$a0, result's address is in \$a1)

```
15 ple -> [char A[4] = {1, 2, 3, 4};
45 ye (wwb) int result;
              result = A[0] + A[1] + A[2] + A[3];
              16 660, 1 (5ap)
              16 stz, 2(60,9)
               16 5t3, 3($ad)
              add 150, 5to, 5t2
add 15to, 5to, 5t3
Sw March 150, 0 ($91)
```

kaz INT A [4], AZOJ Ø(593) AZJ 9(\$93) A[2]8(503) At 3] 12(5a3) 8