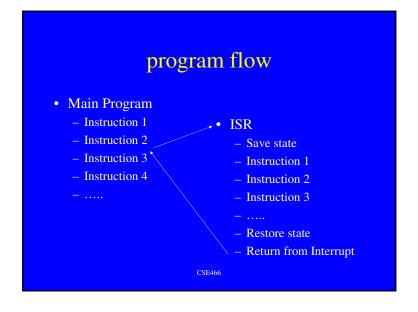
Interrupts CSE466

What is an Interrupt?

- Reaction to something in I/O
- Asynchronous in nature
- Invokes Interrupt handler, or ISR

CSE46



Saving and Restoring the context

- Processor and compiler dependant
- Must ensure that registers are saved
- Must save return vector
- Must restore state

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Disabling Interrupts

- Disable instruction
- Priority interrupts
 - Higher priority can interrupt
 - Lower priority can't
- Non-maskable interrupts
- Does the AVR have Priority or non-maskable interrupts?

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More Questions

- If interrupts happen at the same time, which ISR does the processor execute?
- Can one interrupt request signal interrupt another interrupt routine?

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Questions about Interrupts

- How does the processor find the ISR?
- How does it know where the table is?
- Can an ISR be interrupted in the middle of an instruction?

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Disabling Questions...

- What happens to interrupts that occur while interrupts are disabled?
- What if I disable interrupts and forget to reenable them?
- Can I disable or enable them twice?
- What about start-up?

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