Intel® Mote 2 Engineering Platform

DATA SHEET

Rev2.0

Applications

The Intel Mote 2 is an advanced sensor network node platform designed for demanding wireless sensor network applications requiring high CPU/DSP and wireless link performance and reliability. Target applications include industrial vibration, structural monitoring, acoustic and visual monitoring.

Features

- **PXA271 XScale® processor @ [13–416] MHz**
- **Wireless MMX coprocessor**
- **256kB SRAM, 32MB FLASH, 32MB SDRAM**
- **Integrated 802.15.4 radio, support for external radios through SDIO and UART**
- **Integrated 2.4GHz antenna**
- **Multicolor status indicator LED**
- **Basic and advanced expansion connectors supporting : 3xUART, I2C, 2xSPI, SDIO, I2S, AC97, USB host, Camera I/F, GPIO**
- **Mini-USB port for direct PC connection**
- **Compact size 36x48 mm**

Top

Bottom

Description

The Intel Mote 2 is an advanced wireless sensor node platform. The platform is built around a low power XScale processor, PXA271. It integrates an 802.15.4 radio (ChipCon 2420) and a built in 2.4 GHz antenna. It exposes a “basic sensor board” interface, consisting of two connectors on one side of the board, and an “advanced sensor board” interface, consisting of two high density connectors on the other side of the board. The Intel mote 2 is a modular stackable platform and can be stacked with sensor boards to customize the system to a specific application, along with a “power board” to supply power to the system.

Processor

The Intel Mote 2 contains the PXA271 processor. This processor can operate in a low voltage (0.85V) and a low frequency (13 MHz) mode, hence enabling low power operation. The frequency can be scaled to 104 MHz at the lowest voltage level, and can be increased up to 416MHz with Dynamic Voltage Scaling. The processor has many low power modes, including sleep and deep sleep modes. It also integrates 256 KB of SRAM divided into 4 equal banks of 64 KB. The PXA271 is a multi-chip module that includes three chips in a single package, the processor, 32 MB SDRAM and 32 MB of flash. The processor integrates many I/O options making it extremely flexible in supporting different sensors, A/Ds, radio options, etc. These I/O options include I2C, 3 Synchronous Serial Ports one of which dedicated to the radio, 3 high speed UARTs, GPIOs, SDIO, USB client and host, AC97 and I2S audio codec interfaces, fast infrared port, PWM, Camera Interface and a high speed bus (Mobile Scaleable Link). The processor also adds many timers and a real time clock. The PXA271 also includes a wireless MMX coprocessor to accelerate multimedia operations. It adds 30 new media processor instructions, support for alignment and video operations and compatibility with Intel MMX and SSE integer instructions. For more information on the pxa271, check the processor data sheet at http://www.intel.com/design/pca/prodbref/253820.htm

Radio and Antenna

The Intel Mote 2 integrates an 802.15.4 radio transceiver from ChipCon (CC2420). 802.15.4 is an IEEE standard describing the physical & MAC layers of a low power low range radio, aimed at control and monitoring applications. The CC2420 supports a 250 kb/s data rate with 16 channels in the 2.4 GHz band. The Intel Mote 2 platform integrates a 2.4 GHz surface mount antenna which provides a nominal range of about 30 meters. If a longer range is desired, an SMA connector can be soldered directly to the board to connect to an external antenna. Other external radio modules such as 802.11 and Bluetooth can be enabled through the supported interfaces (SDIO, UART, SPI, etc).

Power Supply Solution

To supply the processor with all the required voltage domains, the Intel Mote 2 includes a Power Management IC. This PMIC supplies 9 voltage domains to the processor in addition to the Dynamic Voltage Scaling capability. It also includes a battery charging option and battery voltage monitoring. Two of the PMIC voltage regulators (1.8 V & 3.0 V) are used to supply the sensor boards with the desired regulated supplies at a maximum current of 200 mA. The processor communicates with the PMIC over a dedicated I2C bus (PWRI2C). The Intel Mote 2 platform was designed to support primary and rechargeable battery options as described below, in addition to being powered via USB. The following figure shows how the different battery boards and on board connectors can be used to power the mote.

- Primary Battery

The Intel Mote 2 platform can be powered using primary batteries with a voltage range of 3.2 - 4.5 V (e.g. 3 AAA alkaline batteries). A battery board with a basic or advanced set of connectors can be connected to the Vbat pins of the connector. As shown in the figure below, a diode and fuse should be connected between the battery and mote board to protect the battery and the PMIC.

- Rechargeable Battery

A rechargeable battery can be used to supply power to the Intel Mote 2 platform by connecting it directly to the Vbat pin on the connector. In this case, the PMIC battery charger can be used to recharge the batteries. The battery board should drive the nCHARGE_EN pin low to connect the USB input to the PMIC charger pin, hence allowing to recharge the battery using USB. The PMIC supports single cell Li-Ion at 4.1 and 4.2 V, in addition to a Li-Polymer pack. See the figure below for more details.

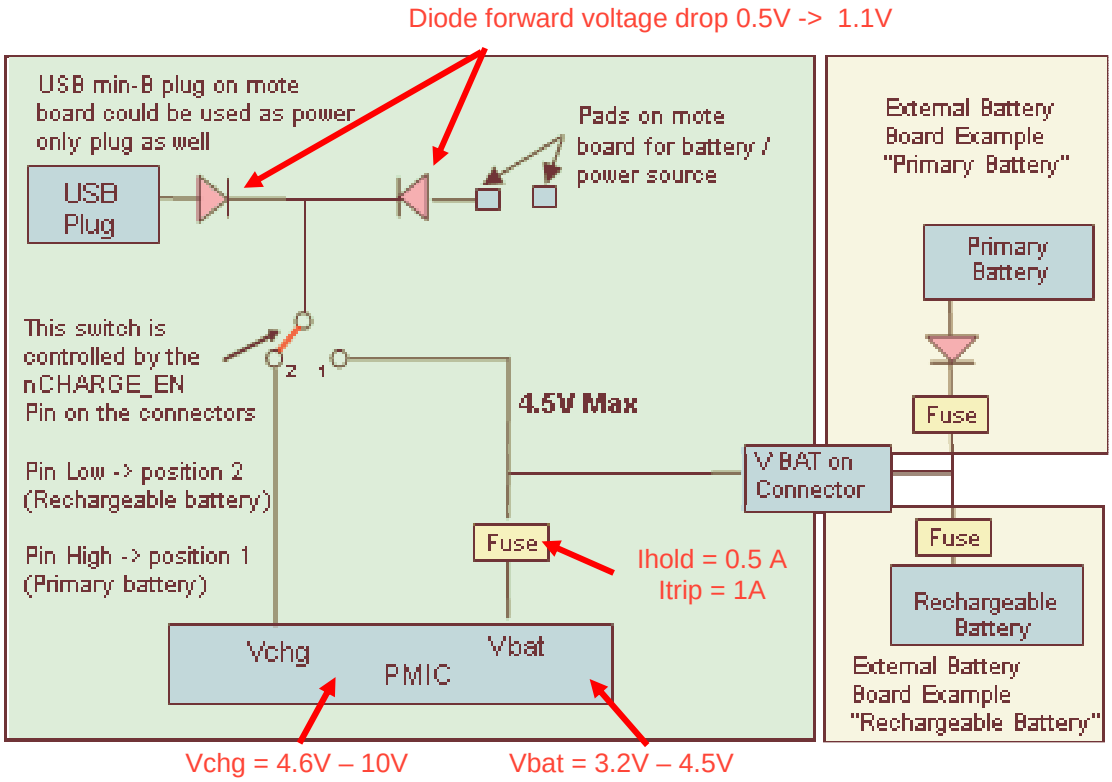
- Mini-USB connector input

The mote can be powered directly from USB, by routing the USB power to the Vbat input of the PMIC. This is the default state when either a battery is not connected, or when a battery board drives the nCHARGE_EN input high (as the case with all primary battery boards). If a battery board pulls nCHARGE_EN low, the USB input gets routed to the Vchg pin of the PMIC, which would be the case for rechargeable batteries as mentioned above.

- On-board pads

The On board pads can be used to connect a primary battery directly to the mote. A diode is included in this path to protect the primary battery. In addition, these pads can be used to connect any power source supplying a voltage range of 3.2 – 4.5V (after the diode drop). This connector is similar to the USB connector functionality, as it could be used to supply power to the mote or to recharge a battery based on the state of the nCHARGE_EN pin.

The PMIC is also used to enable the alarm functionality that is exposed on the basic and advanced sensor connectors. When power is supplied to the mote, the PMIC will start, however it will not start the mote until the power button is pushed (similar to a cell phone usage model). If it is desired to have a power board automatically turn on the mote, the power board can short the alarm pin on the connector to the VRTC pin. This will cause the mote to start automatically every time power is applied to the mote. However, if a more intelligent sensor board is desired to start the mote in response to a specific sensor event, the alarm pin can be controlled by the sensor board to start/wakeup the mote selectively.



Sensor Board Interfaces

The Intel Mote 2 platform exposes 2 sets of connectors, the basic set and the advanced set. The pins on each connector set are split into two physical connectors to enhance the mechanical stability. The basic set is meant to enable low cost sensor boards (low density connectors were chosen) and support the most common sensor interfaces. This connector set is defined as the “architectural” set, and can be supported in future mote designs. The advanced connector set exposes some of the PXA271 advanced features (Camera Interface, High speed bus, Audio interfaces, etc), and is assumed to be platform specific. The details of the connector sets are described below.

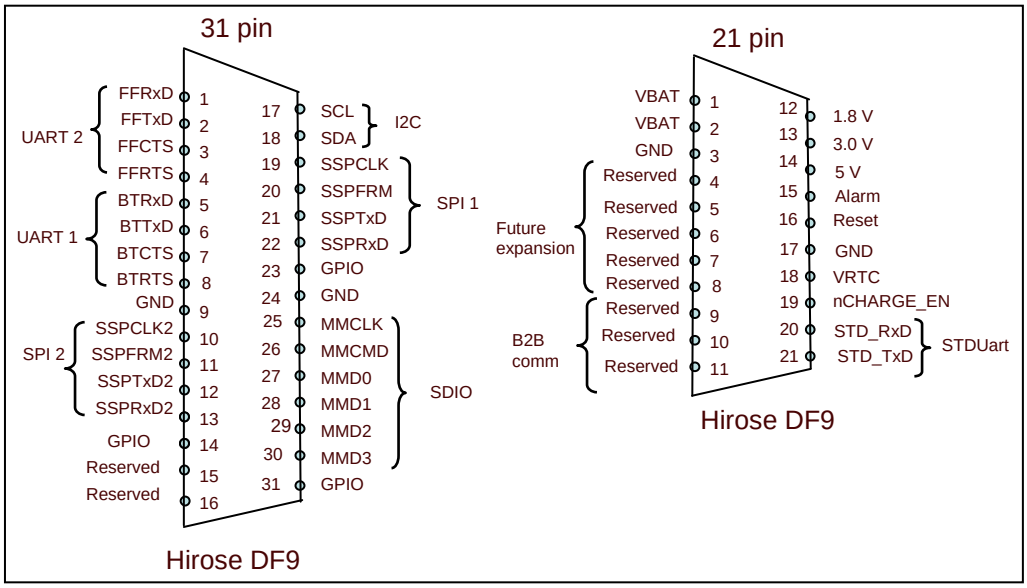
- **Basic Connector Set**

The basic connector set consists of 2 physical connectors from the Hirose DF9 family which has a 1 mm pitch. The connector choice simplifies the routing and soldering of sensor boards, which is useful in the prototyping stage. The pins are split between the 2 connectors (31 pin and 21 pin connectors) for mechanical stability reasons. The asymmetry of the two connectors provides a useful visual clue of sensor board orientation. All I/O pins can be programmed as GPIOs in addition to their special port function. As mentioned in the power supply section, the 1.8 and 3.0 V pins are supplied by the PMIC and can be used to power the sensor boards. The alarm pin is an input pin and can be used by the sensor boards to wake up the processor out of deep sleep mode if needed. The reset pin is an input pin to force a hardware reset of the processor. The standard UART will be used as the debug console and is exposed on the 21 pin connector. The 31 pin connector exposes 2 high speed UART ports, 2 SSP ports, an SDIO port, an I2C port and multiple GPIOs. There are 11 reserved pins to allow for future expansion and inter-board communication.

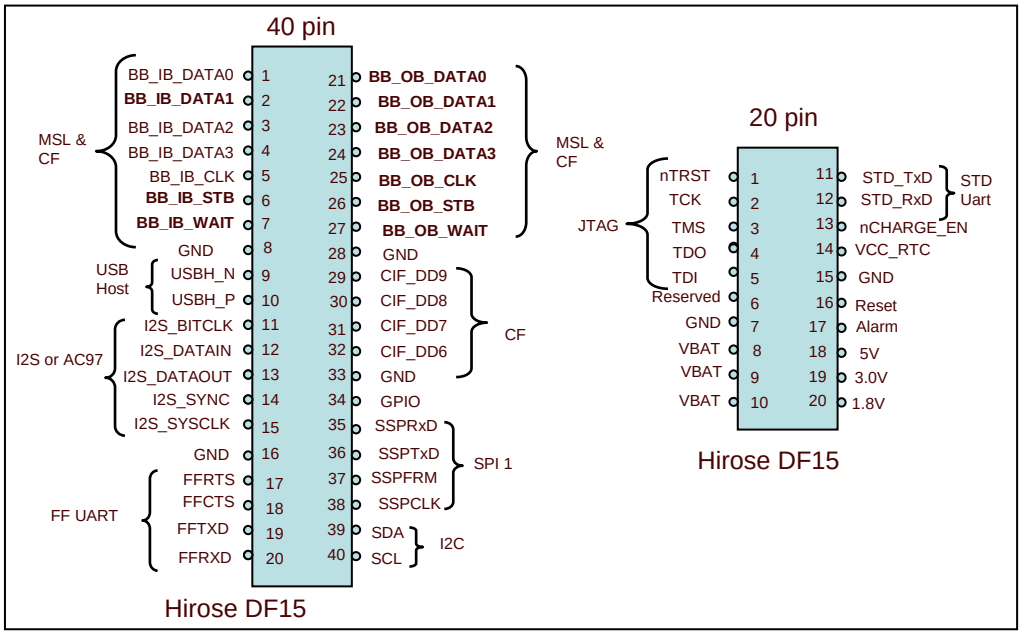
- **Advanced Connector Set**

The advanced connector set also consists of 2 physical connectors. We chose a higher density connector (0.65mm pitch) for the advanced set to be able to support the large pin count required without increasing the size of the connector too much. The pins are split on 2 connectors (40 pin and 20 pin connectors) for mechanical stability reasons. Note that all I/O pins (with the exception of JTAG and USB) can be programmed as GPIOs in addition to their special port function. JTAG is exposed on the 20 pin connector. The MSL interface provides two independent high speed unidirectional links. The data-channel width can

be scaled from 1 to 4 bits, providing up to 192 Mbps at 48 MHz. The CIF port supports the Intel Quick Capture Camera Interface, to easily attach image sensors to the Intel Mote 2. Note that the I^2C, UART and SPI ports exposed on the 40 pin connector, are the same ports exposed on the basic side.



Basic Connector Set



Advanced Connector Set

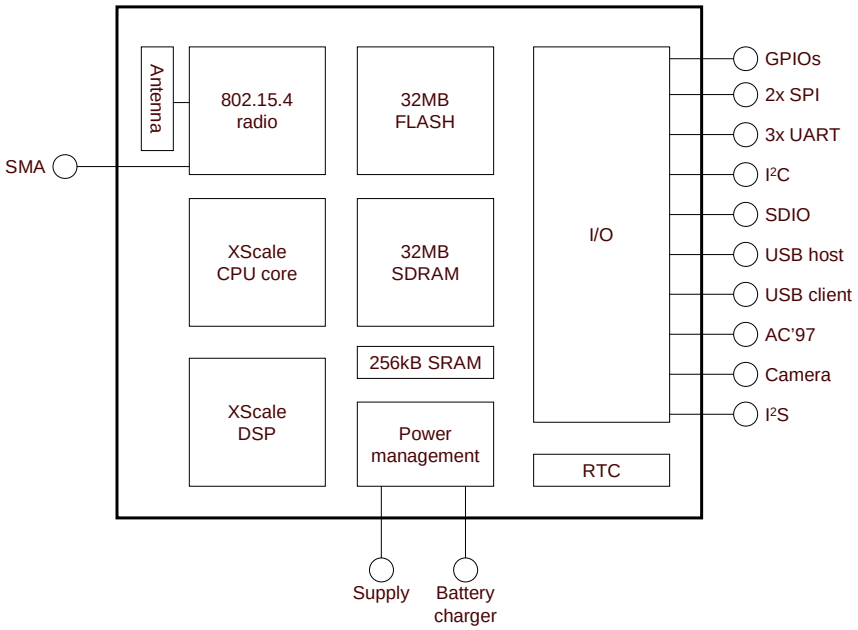
OS Choices

The Intel Mote 2 supports a variety of OS options. Ports of TinyOS 1.1 and 2.0 are available on sourceforge (http://sourceforge.net/projects/tinyos) for extremely low power sensor network applications. A detailed installation manual is provided with this datasheet. In addition, a linux port can be found at http://platformx.sourceforge.net for more advanced applications.

Board Revision

This datasheet corresponds to Rev 2.0 of the Intel Mote 2 platform. This revision has serial numbers in the range of 0x00003000 – 0x00003FFF

Block diagram



Absolute maximum ratings

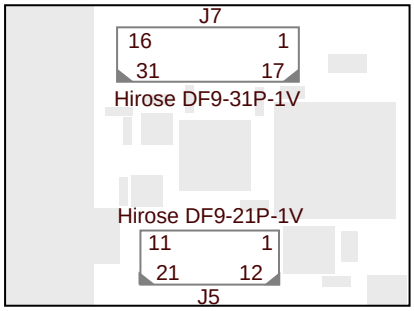
Supply voltage	V_{batt}	5.5	V
Charger input voltage	V_{chg}	10	V
Input voltage	V_{in}	$V_{CC\ IO}$ ± 0.3	V
Storage temperature	T_s	-40 - 125	ºC

Operating conditions

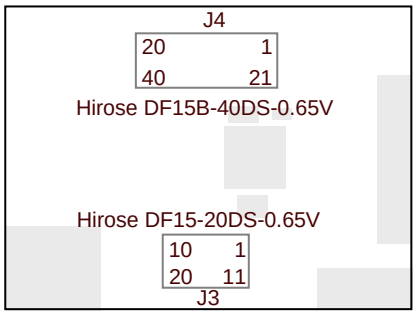
Temperature range	T_o	0 - 85	ºC
Current in deep sleep mode	I_{sleep}	387	uA
Current in active mode (13 MHz, radio off)	I_{avg1}	31	mA
Current in active mode (13 MHz, radio Tx/Rx)	I_{avg2}	44	mA
Current in active mode (104 MHz, radio Tx/Rx)	I_{avg3}	66	mA

Connector information

Top



Bottom



Top Side: Large connector (J7)

Pin#	Type	Name	GPIO#	Description
1	I/O	FF_RXD	96	UART 1 receive data
2	I/O	FF_TXD	99	UART 1 send data
3	I/O	FF_CTS	100	UART 1 clear to send
4	I/O	FF_RTS	98	UART 1 request to send
5	I/O	BT_RXD	42	UART 2 receive data
6	I/O	BT_TXD	43	UART 2 send data
7	I/O	BT_CTS	44	UART 2 clear to send
8	I/O	BT_RTS	45	UART 2 request to send
9		GND		Ground
10	I/O	SSP2_SCLK	36	Synchronous Serial Port 2 clock
11	I/O	SSP2_SFRM	37	Synchronous Serial Port 2 frame
12	I/O	SSP2_TXD	38	Synchronous Serial Port 2 transmit data
13	I/O	SSP2_RXD	11	Synchronous Serial Port 2 receive data
14	I/O	GPIO94	94	General purpose I/O
15	*R*	*Reserved*		*Do not connect*
16	*R*	*Reserved*		*Do not connect*
17	I/O	I2C_SCL	117	I2C serial clock
18	I/O	I2C_SDA	118	I2C serial data/address bus
19	I/O	SSP1_SCLK	23	Synchronous Serial Port 1 clock
20	I/O	SSP1_SFRM	24	Synchronous Serial Port 1 frame
21	I/O	SSP1_TXD	25	Synchronous Serial Port 1 transmit data
22	I/O	SSP1_RXD	26	Synchronous Serial Port 1 receive data
23	I/O	GPIO10	10	General purpose I/O
24		GND		Ground
25	I/O	MM_CLK	32	MMC and SD/SDIO bus clock
26	I/O	MM_CMD	112	MMC and SD/SDIO command
27	I/O	MM_DAT0	92	MMC and SD/SDIO read / write data 0
28	I/O	MM_DAT1	109	MMC and SD/SDIO read / write data 1
29	I/O	MM_DAT2	110	MMC chip select 0 or SD/SDIO read / write data 2
30	I/O	MM_DAT3	111	MMC chip select 1 or SD/SDIO read / write data 3
31	I/O	GPIO93	93	General purpose I/O

Top Side: Small connector (J5)

Pin#	Type	Name	GPIO#	Description
1		VBAT		Power Supply Rail (3.2 – 4.7 V minus Diode Drop)
2		VBAT		Power Supply Rail (3.2 – 4.7 V minus Diode Drop)
3		GND		Ground
4	R	*Reserved*		*Do not connect*
5	*R*	*Reserved*		*Do not connect*
6	*R*	*Reserved*		*Do not connect*
7	*R*	*Reserved*		*Do not connect*
8	*R*	*Reserved*		*Do not connect*
9	R	N/C		Available for communication between expansion boards
10	R	N/C		Available for communication between expansion boards
11	R	N/C		Available for communication between expansion boards
12		VCC_1P8		1.8 V supply rail to power sensor boards
13		VCC_3V		3.0 V supply rail to power sensor boards
14	*R*	*Reserved*		*Do not connect*

15		ALARM		Alarm input to PMIC (see power subsystem)
16		NRESET		Reset processor signal
17		GND		Ground
18		VCC_RTC		Power supply for the RTC voltage domain of the PXA
19		VCC_IO		Power supply for the IO voltage domain of the PXA
20	I/O	STD_RXD	46	UART 3 receive data
21	I/O	STD_TXD	47	UART 3 send data

Bottom Side: Large connector (J4)

Pin#	Type	Name	GPIO#	Description
1	I/O	BB_IB_DATA0 CIF_DD5	82	MSL inbound data bit 0 Quick capture data line 5
2	I/O	BB_IB_DATA1 CIF_DD1	55	MSL inbound data bit 1 Quick capture data line 1
3	I/O	BB_IB_DATA2	56	MSL inbound data bit 2
4	I/O	BB_IB_DATA3	57	MSL inbound data bit 3
5	I/O	BB_IB_CLK CIF_DD4	83	MSL inbound clock strobe Quick capture data line 4
6	I/O	BB_IB_STB CIF_FV	84	MSL inbound signal qualifier Quick capture frame start
7	I/O	BB_IB_WAIT CIF_LV	85	MSL wait indicator for inbound link Quick capture line start
8		GND		Ground
9		USBH_N_CONN		Data negative differential signal (USB D-)
10		USBH_P_CONN		Data positive differential signal (USB D+)
11	I/O	I2S_BITCLK AC97_BITCLK	28	I2S bit clock, supplies the serial audio bit rate AC97 12.288-MHz bit-rate clock
12	I/O	I2S_DATA_IN AC97_SDATA_IN_0	29	I2S Serial audio input data from CODEC AC97 Serial audio input data from CODEC
13	I/O	I2S_DATA_OUT AC97_SDATA_OUT	30	I2S Serial audio output data to CODEC AC97 Serial audio output data to CODEC
14	I/O	I2S_SYNC AC97_SYNC	31	I2S SYNC, BITCLCK divided by 64 AC97 48-KHz frame indicator and synchronizer
15	I/O	I2S_SYSCLK AC97_RESET_n	113	I2S system clock = BITCLK x 4 AC97 CODEC reset
16		GND		Ground
17	I/O	FF_RTS	98	UART 1 request to send
18	I/O	FF_CTS	100	UART 1 clear to send
19	I/O	FF_TXD	99	UART 1 send data
20	I/O	FF_RXD	96	UART 1 receive data
21	I/O	BB_OB_DATA0 CIF_DD0	81	MSL outbound data bit 0 Quick capture data line 0
22	I/O	BB_OB_DATA1 CIF_DD5	48	MSL outbound data bit 1 Quick capture data line 5
23	I/O	BB_OB_DATA2 CIF_DD3	50	MSL outbound data bit 2 Quick capture data line 3
24		BB_OB_DATA3 CIF_DD2	51	MSL outbound data bit 3 Quick capture data line 2
25	I/O	BB_OB_CLK CIF_DD4	52	MSL outbound clock strobe Quick capture data line 4
26	I/O	BB_OB_STB CIF_MCLK	53	MSL outbound signal qualifier Quick capture programmable output clock
27	I/O	BB_OB_WAIT CIF_PCLK	54	MSL wait indicator for outbound link Quick capture pixel clock

28		GND		Ground
29	I/O	CIF_DD9	106	Quick capture data line 9
30	I/O	CIF_DD8	107	Quick capture data line 8
31	I/O	CIF_DD7	12	Quick capture data line 7
32	I/O	CIF_DD6	17	Quick capture data line 6
33		GND		Ground
34	I/O	GPIO10	10	General purpose I/O
35	I/O	SSP1_RXD	26	Synchronous Serial Port 1 receive data
36	I/O	SSP1_TXD	25	Synchronous Serial Port 1 transmit data
37	I/O	SSP1_SFRM	24	Synchronous Serial Port 1 frame
38	I/O	SSP1_SCLK	23	Synchronous Serial Port 1 clock
39	I/O	I2C_SDA	118	I2C serial data
40	I/O	I2C_SCL	117	I2C serial clock

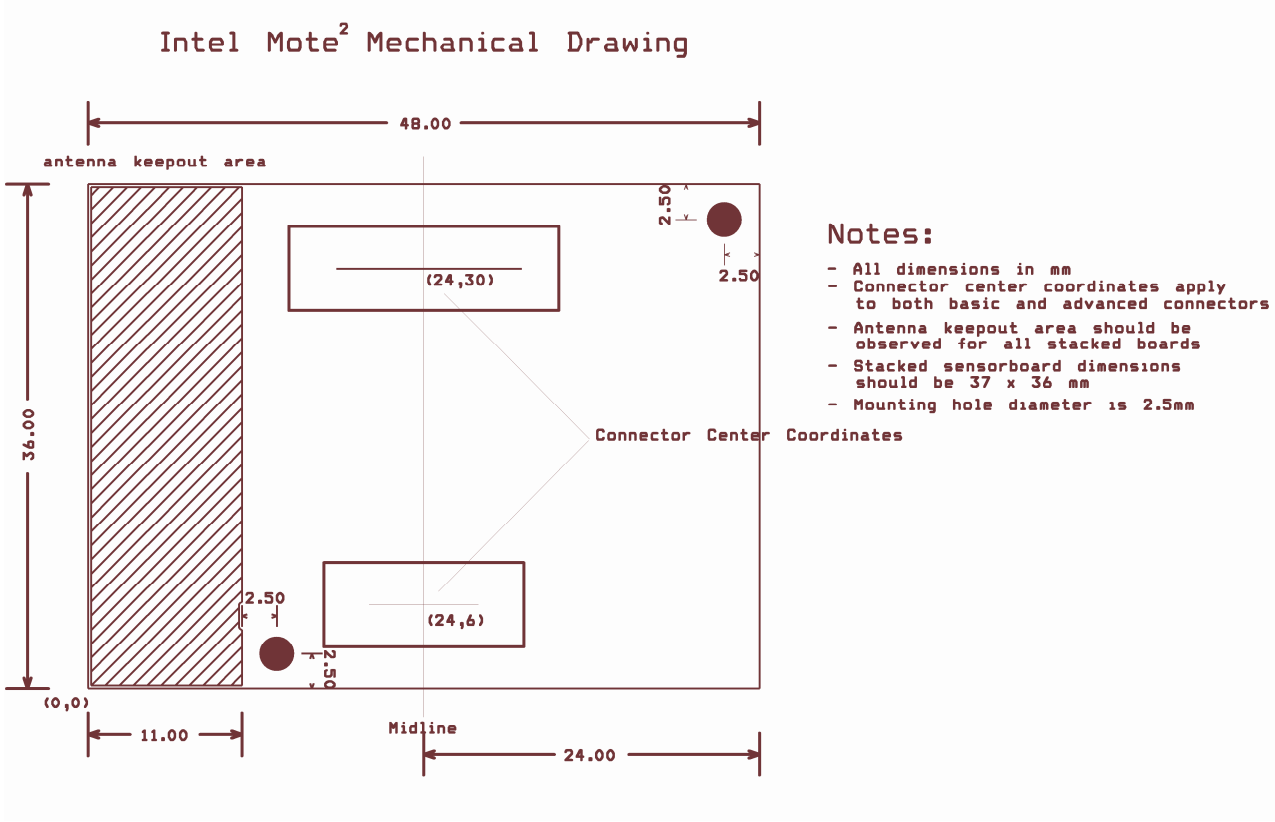
Bottom Side: Small connector (J3)

Pin#	Type	Name	GPIO#	Description
1		JTAG_NTRST		JTAG port : Test Reset
2		JTAG_TCK		JTAG port : Test clock
3		JTAG_TMS		JTAG port : Test mode select
4		JTAG_TDO		JTAG port : Test data out
5		JTAG_TDI		JTAG port : Test data in
6	*R*	*Reserved*		*Do not connect*
7		GND		Ground
8		VBAT		Power Supply Rail (3.2 – 4.7 V minus Diode Drop)
9		VBAT		Power Supply Rail (3.2 – 4.7 V minus Diode Drop)
10		VBAT		Power Supply Rail (3.2 – 4.7 V minus Diode Drop)
11		STD_RXD		UART 3 receive data
12		STD_TXD		UART 3 send data
13		VCC_IO		Power supply for the IO voltage domain of the CPU
14		VCC_BAT_RTC		Power supply for the RTC voltage domain of the CPU
15		GND		Ground
16		NRESET		Reset processor
17		ALARM		Alarm input to PMIC (see power subsystem)
18		VCC_5V		5.0 V supply rail to power sensor board (USBH)
19		VCC_3V		3.0 V supply rail to power sensor boards
20		VCC_1P8		1.8 V supply rail to power sensor boards

Internal I/O configuration

Component	Pin name	GPIO#
LED	Red	103
LED	Green	104
LED	Blue	105
CC2420	FIFO	114
CC2420	VREG_EN	115
CC2420	CCA	116
CC2420	FIFOP	0
CC2420	RESETN	22
CC2420	SFD	16

Mechanical Specifications



Matching connector information

Description	Manufacturer	Part#
40 pin (bottom)	Hirose	DF15B(3.2)-40DP-0.65V
20 pin (bottom)	Hirose	DF15B(3.2)-20DP-0.65V
31 pin (top)	Hirose	DF9-31S-1V
21 pin (top)	Hirose	DF9-21S-1V

Connector notes: The Hirose DF15 connector type comes in wide variety of stacking heights. Using the recommended part numbers will result in a 5mm stacking height on the bottom side. If desired, an expansion board designer can choose a different part number of the DF15 connector used in order to meet custom stacking height requirements.