Multiple Instruction Issue

Multiple instructions issued to FUs each cycle

- a processor that can execute more than one instruction per cycle
- **issue width** = the number of **issue slots**, 1 slot/instruction
- not all types of instructions can be issued together
  - an example: 2 ALUs, 1 load/store unit, 1 FPU
    1 ALU does shifts & integer multiplies; the other executes branches

Superscalars

Performance impact: increase instruction throughput

- execute multiple instructions in parallel, not just overlapped
  - CPI potentially < 1 (.25 if 4-wide)
  - IPC (instructions/cycle) potentially > 1 (4 if 4-wide)
- better functional unit utilization

Multiple Instruction Issue on Superscalars

Requires:

- instruction fetch
  - fetch of multiple instructions at once
  - sophisticated dynamic branch prediction
  - prefetch speculatively beyond conditional branches
- instruction issue
  - determine which instructions can be issued next
  - choose which of ready instructions to issue
  - issue multiple instructions in parallel
- execution
  - multiple functional units
- instruction commit
  - commit several instructions in fetch order

Duplicate & more complex hardware, potentially longer wires

Superscalars

Hardware impact:

- more & pipelined functional units
- multi-ported registers for multiple register access
- more buses from the register file to the additional functional units
- multiple decoders
- more hazard detection logic
- more bypass logic
- wider instruction fetch
- multi-banked L1 data cache

or else the processor has structural hazards (due to an unbalanced design) and stalling

There are restrictions on instruction types that can be issued together to reduce the amount of hardware.

Static (compiler) scheduling helps.

Superscalars

Requires:

- need independent instructions
- need a good local mix of instructions
- need more instructions to hide load delays

Harder code scheduling job for the compiler

Multiple Instruction Issue

Scheduling instructions:

- which instructions are sent to the functional units for execution & when
- schedule for available FUs & to hide latency

Superscalar processors

- instructions are scheduled for execution ***by the hardware***
- ***different*** numbers of instructions may be issued at once

VLIW ("very long instruction word") **processors**

- instructions are scheduled for execution ***by the compiler***
- a ***fixed*** number of operations are formatted as one big instruction
- usually **LIW** (3 operations) today