Topics

ILP & TLP

Multiprocessors
- Cache coherency on bus-based & distributed MIMDs
- Synchronization

Multithreaded processors
- Traditional vs. SMT

Dataflow machines

Themes Throughout Different Designs

Uses of snooping
Distributed implementations
Mechanisms for increasing throughput of something
Motivation for the different designs
How different processor designs achieved their goals
Why different designs work well
Different scenarios for speculation
State bits for cache blocks
Different scenarios for out-of-order execution
Designs that have changed the ISA