More Embedded Microcontrollers

- Motorola 68HC11
- Microchip PIC
- Motorola 683xx
- Motorola 68328
- Intel i960
- Motorola MPC823
- Motorola ColdFire

Motorola 68HC11

- Motorola 68HC11 (A1 model)
  - 8-bit microcontroller with a M6800/M6801 processor core
  - on-board 512-byte EEPROM and 256-byte RAM
  - 16-bit timer system with input capture and output compare
  - built-in A/D converter for 8 analog inputs
  - serial communications interfaces
- Development board for 68HC11 (M68HC11EVB)
  - 68HC11A1 system with 8K user EPROM and up to 16K user RAM
  - port replacement unit
    - to regain I/O ports used for memory addressing
  - two serial communications interfaces
  - on-board monitor program for downloading and debugging programs
    - includes basic I/O utilities

MC68HC11 and EVB

- Review manuals
  - learn how to read documentation
- Instruction set
  - instruction capabilities
  - timing
- Special registers and integrated I/O devices
  - input capture
  - output compare
  - analog/digital conversion
- Interrupt organization
- Memory space and its allocation
- Timers

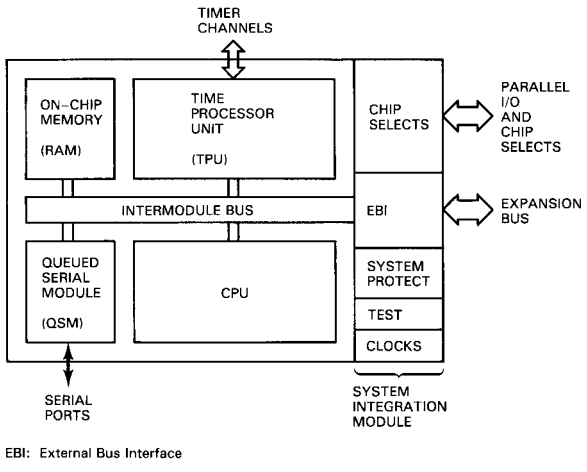
Small microcontrollers

- 68HC11
  - basic microcontroller with simple instruction set
  - full-featured (many of the same features as larger microcontrollers)
  - good real-time capabilities
  - A/D conversion built-in
  - cheap
  - very common (lots of resources available including on web)
  - public domain C compiler available
  - evaluation board with debugging support (BUFFALO ROM)
- PIC (Microchip)
  - small footprint (as few as 24 pins)
  - no external system bus
  - lots of members of family differentiated by I/O pin capabilities
    - A/D, serial I/O, interrupts, input capture, etc.

Motorola MC683xx

- Designed by Motorola for automotive, data acquisition, printers, plotters, cameras, and other consumer products
- Introduced in 1989 (9 years ago)
- General characteristics
  - operate in harsh environment (-40 to 125°C and noise)
  - low power (~625mW), low cost ~$12
  - crunch numbers (execute control loops)
  - clock frequency (up to 78MHz)
- Functional units
  - CPU32 (68020 processor core)
  - SIM (System Integration Module)
  - GPT (General Purpose Timer)
  - QSM (Queued Serial Module)
  - TPU (Time Processor Unit)

Block diagram



Functional blocks

- CPU32
  - 32-bit processor based on 68020
- System Integration Module
  - controls external bus, I/O functions and system clock
- Time Processor Unit
  - 16-channel timer/counter unit
  - controls internal/external events
- Memory Module
  - on-chip RAM with stand-by power feature
- A/D
  - 16 channel queued
- CAN protocol
  - Controller Area Network (automotive bus protocol)

Time Processor Unit

- A microcontroller dedicated to timing control
- Two 16-bit timers/registers
  - free running based on system clock
  - can be controlled with external clock
- 16 independent channels (input or output)
- Functions
  - input capture
  - period or pulse width accumulation
  - output compare
  - pulse width modulation
  - stepper motor control
  - automotive functions (fire spark plugs, determine engine rotation)

Clocks and Timers

- System clock
- Periodic interrupt timer
- Software watchdog timer
- Bus monitor
- Synchronous communication
  - baud rate, delay, min idle
- Asynchronous communication baud rate
- TPU timers

MC68328 aka DragonBall (Palm Pilot)

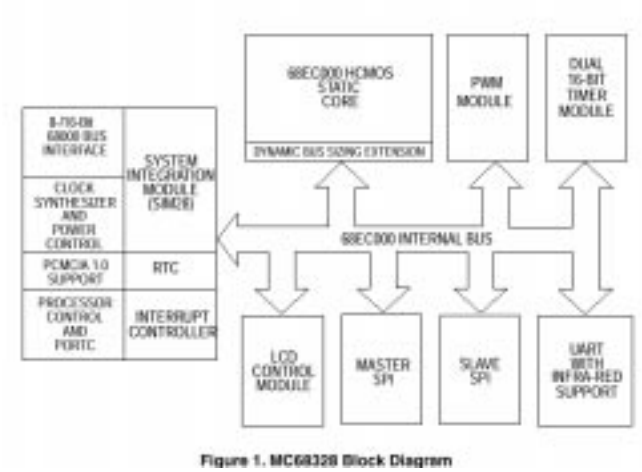


Figure 1. MC68328 Block Diagram

PWM on DragonBall

- PWM transforms duty cycle into an average analog value
- In addition to controlling motor velocity, can synthesize music

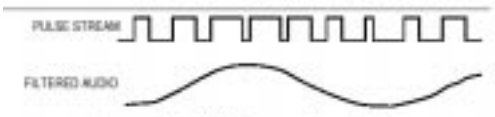


Figure 14-2. PWM Generating Audio

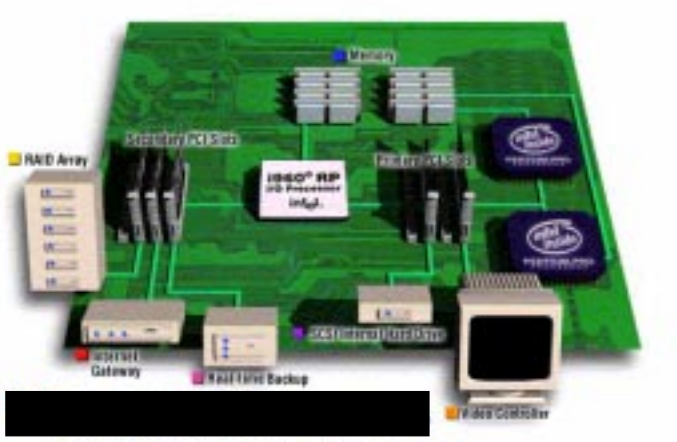
I/O Bottleneck

- Off-chip communication very slow relative to processing speeds
  - processor generating lots of memory requests
  - multiple devices competing for system bus
- Technology wave increasing the gap in performance
  - processors running faster
  - interconnect bandwidth increasing at slower rate
- How do local area networks handle this problem?
  - restrict communication
  - hubs, gateways
- Solution
  - off load communication to a communication processor

Intel's Approach

- A two-pronged attack
  - hardware: communication processor
  - software: device-drivers
- Use a RISC processor to handle communication for the main processor
  - isolate main processor from slower peripherals
  - reduce interrupts to CPU
  - support for system busses running at different clock rates
- Define a new standard: Intelligent I/O
  - standardize device-drivers
  - minimize OS dependencies
  - increase system throughput

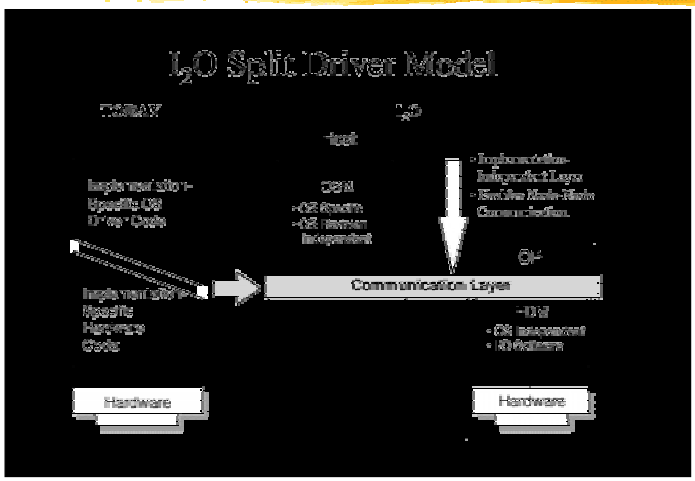
System w/ Communication Processor



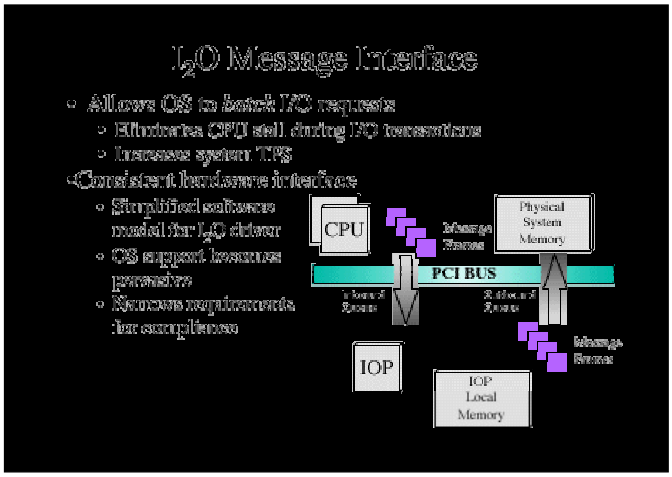
I_2O

- Goals
  - abstract the I/O subsystem
  - improve system throughput
  - enable rapid deployment of new I/O technology
- Message-passing paradigm
  - supports peer communication
  - simplifies device-drivers

I_2O Device-Drivers



I2O Message Passing



Intel i960-RP Processor

- Main features
  - PCI to PCI bridge
  - messaging unit
    - mechanism to transfer data between the PCI system and 80960
  - DMA access to both PCI busses
  - address translation units
    - 64-byte input and output queues
    - queues allow transactions to complete on initiating bus before they complete on target bus
  - 7 to 150 MIPS

i960 Block Diagram

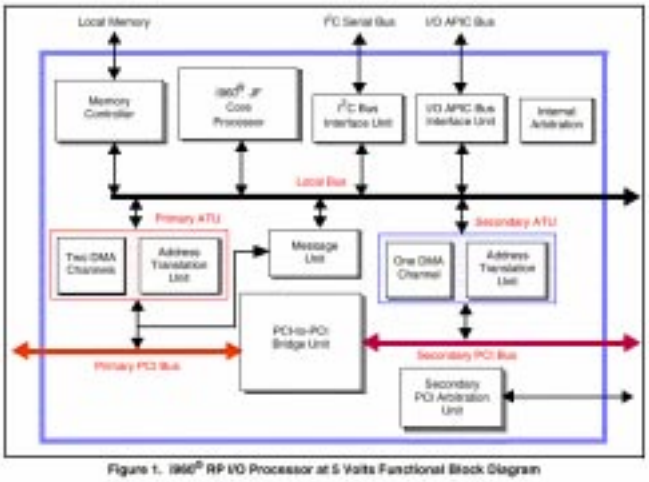


Figure 1. i960® RP I/O Processor at 5 Volts Functional Block Diagram

i960 Messaging Unit

- Message registers
  - i960 sends and receives messages via special registers
  - when written an interrupt generated to i960 or PCI
- Doorbell registers
  - inbound and outbound doorbells
  - either hardware or software can generate doorbell interrupts
  - contain interrupt status from other message unit mechanisms
- Circular queues
  - two inbound and two outbound queues
  - posted messages contain orders
  - free messages indicate operation completed and message can be reused

Motorola's Approach

- Use 2 RISC processors
  - 32-bit PowerPC core for application code
  - 32-bit customized RISC for imaging and communication
- Put communication processor on same die as main processor
  - system on a chip
  - incorporate features common in portable devices
  - single-chip solution for consumer electronics
  - signal processing functions

MPC823

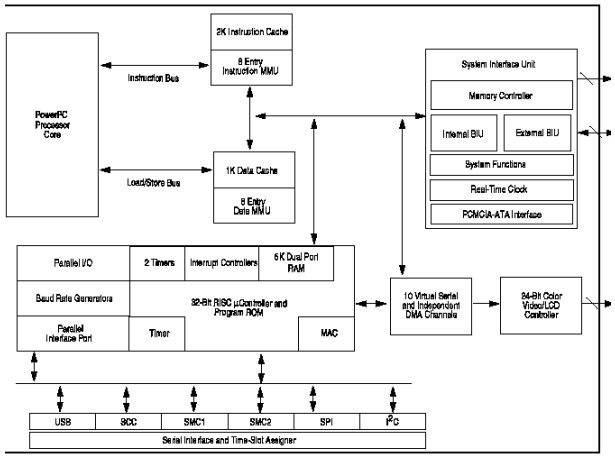


Figure 1. MPC823 Microprocessor Block Diagram

MPC 823 Features

- Performance of 66 MIPS @ 50MHz
- Low power
  - consumes less than 180mW @ 25MHz
  - 2.2V internal, 3.3V I/O boundary
  - doze - functional units disabled except
    - PLL, mem-controller, real-time clock, LCD, comm. proc in standby
  - sleep - all units disabled except
    - real-time clock, periodic interrupt timer, PLL active for fast wakeup
  - deep sleep - all units disabled except
    - real-time clock, periodic interrupt timer
- 1K data cache and 2K instruction cache
- PCMCIA support

Communication Module Features

- Interfaces to PPC core via on-chip dual ported RAM
- Protocols supported include
  - Ethernet/ IEEE 802.3
  - Universal Serial Bus (USB), AppleTalk, UART/USART, I2C
  - IrDA 1.1
  - ISDN
- 16x16 bit multiply accumulate (MAC)
- DSP functions
  - V.32bis/V.34bis datapump filter
  - JPEG compression
- Four independent baud rate generators

More Communication Module Features

- Video/LCD controller
  - supports passive LCD and NTSC/PAL encoders
  - end of frame interrupt generation
  - programmable display active area
  - programmable background color for inactive area
  - 1,2,4-bit per pixel grayscale
  - built-in color RAM with 256 12-bit entries
  - programmable polarity for all LCD interface signals

PDA Based on MPC823

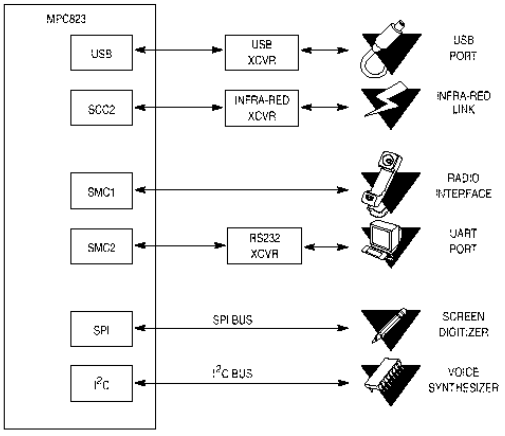
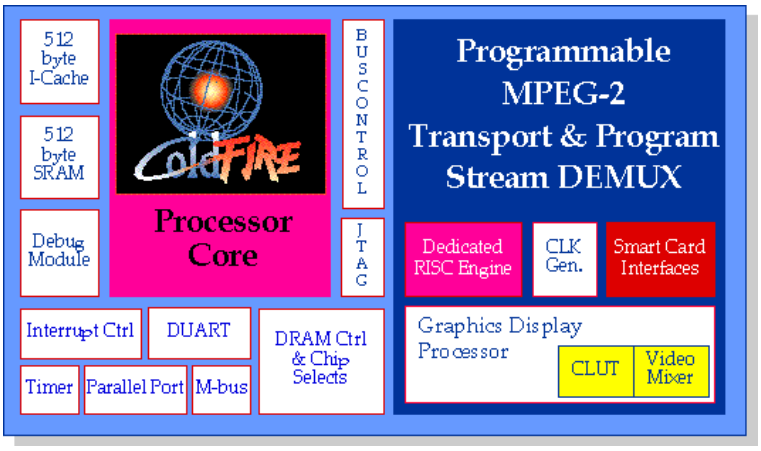


Figure 16-2. Example of a PDA Application

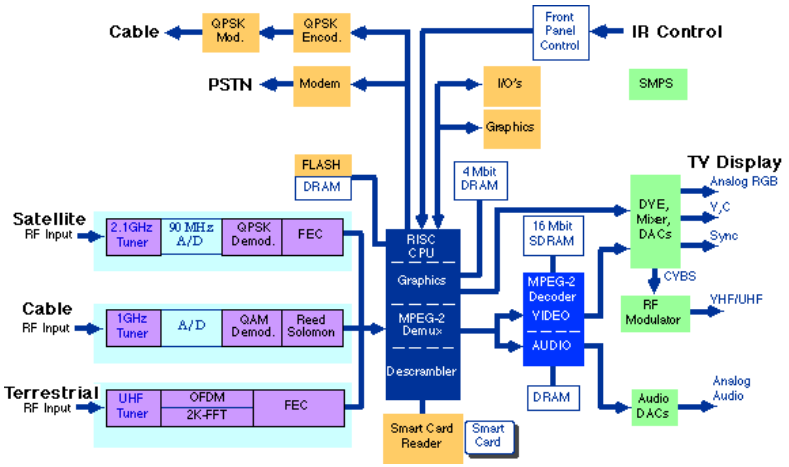
Motorola's ColdFire



ColdFire Features

- Variable instruction length RISC 68K processor
  - subset of 68K instruction set
  - 16, 32, 48-bit instruction sizes
  - single-cycle instruction execution
  - tighter code density than 32 or 64-bit processors
- Completely synthesizable
  - core can be used in system on a chip designs
- Performance: 36 MIPS
- Price: ~$25

Set-Top Box


Cable
QPSK Mod.
QPSK Encod.
Front Panel Control
IR Control
PSTN
Modem
I/O's
SMPS
Graphics
FLASH
DRAM
4 Mbit DRAM
TV Display
Analog RGB
Y,C
Sync
Satellite
RF Input
2.1GHz Tuner
90 MHz A/D
QPSK Demod.
FEC
RISC CPU
Graphics
MPEG-2 Demux
Descrambler
16 Mbit SDRAM
MPEG-2 Decoder
VIDEO
AUDIO
DVE, Mixer, DACs
CVBS
RF Modulator
VHF/UHF
Cable
RF Input
1GHz Tuner
A/D
QAM Demod.
Reed Solomon
DRAM
Audio DACs
Analog Audio
Terrestrial
RF Input
UHF Tuner
OFDM
2K-FFT
FEC
Smart Card Reader
Smart Card