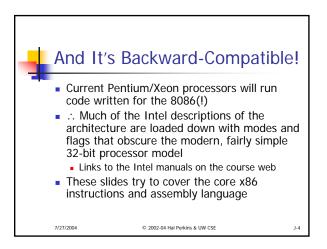
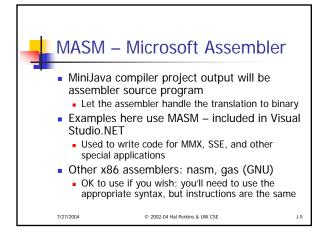
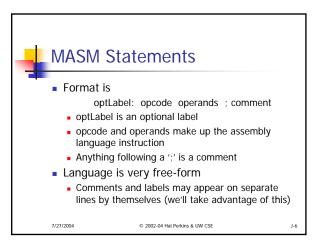
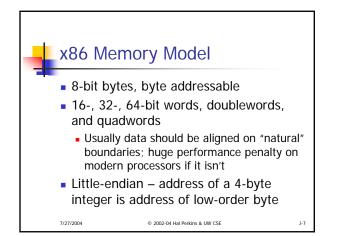


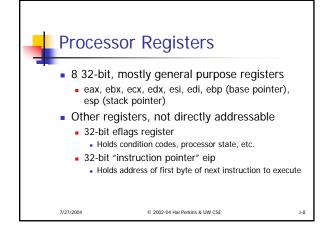
x86 Selected History							
Processor	Intro Year	Intro Clock	Transistors	Features			
8086	1978	8 MHz	29 K	16-bit regs., segments			
286	1982	12.5 MHz	134 K	Protected mode			
386	1985	20 MHz	275 K	32-bit regs., paging			
486	1989	25 MHz	1.2 M	On-board FPU			
Pentium	1993	60 MHz	3.1 M	MMX on late models			
Pentium Pro	1995	200 MHz	5.5 M	P6 core, bigger caches			
Pentium II	1997	266 MHz	7 M	P6 w/MMX			
Pentium III	1999	700 MHz	28 M	SSE (Streaming SIMD)			
Pentium IV	2000	1.5 GHz	42 M	NetBurst core, SSE2			
Xeon	2002	2.2 GHz	55 M	Hyper-Threading			
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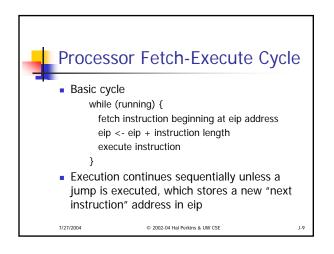


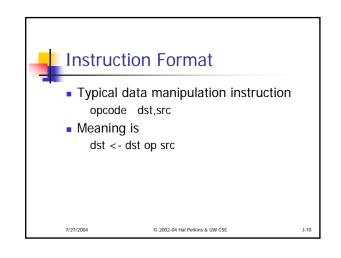


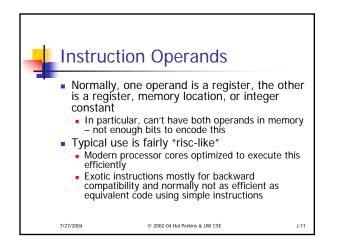


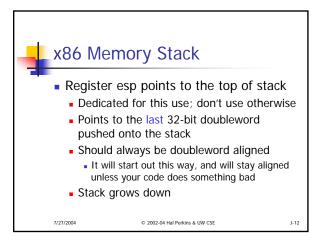


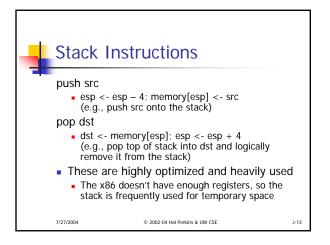


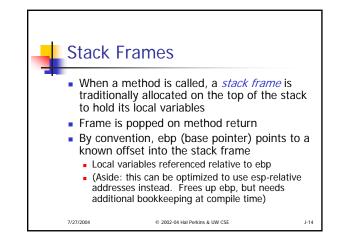


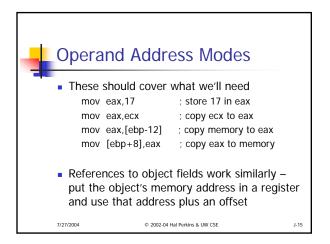


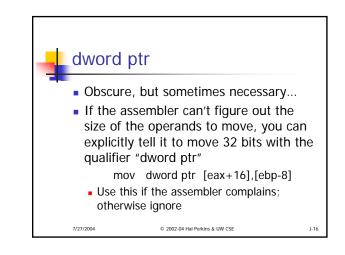


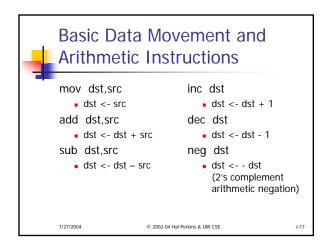


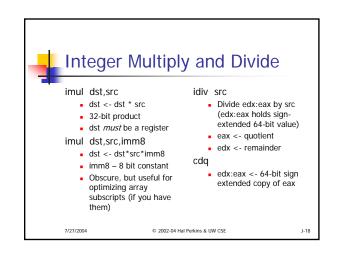


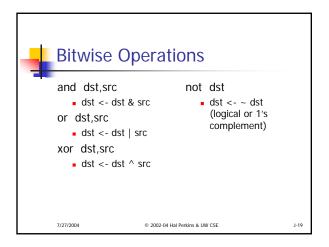


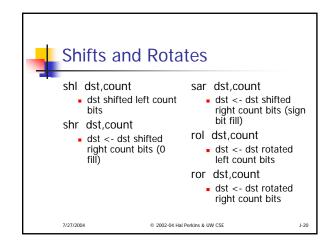


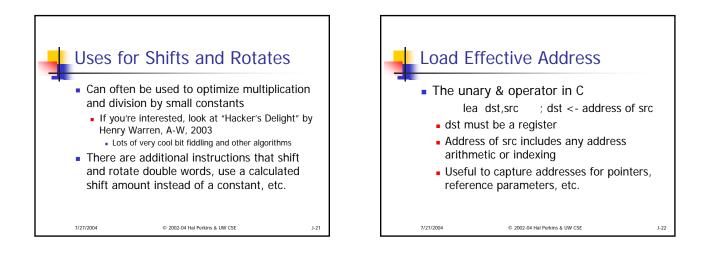


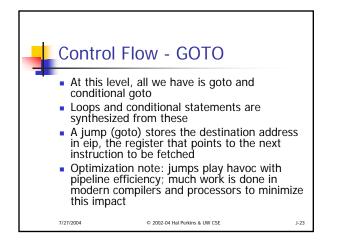


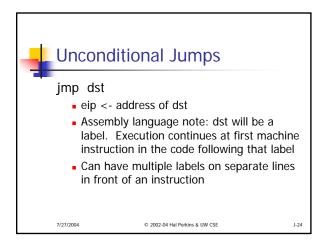


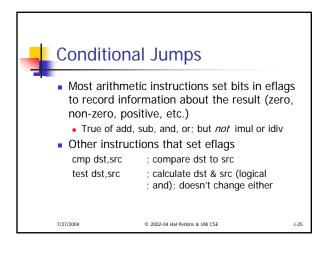




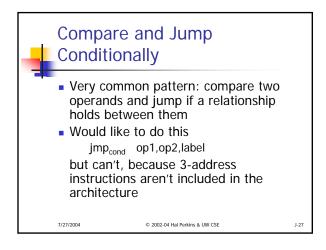


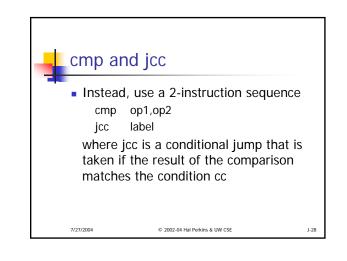


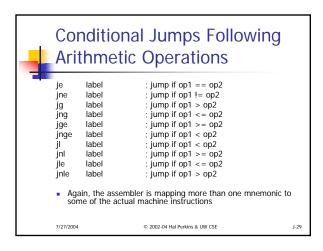


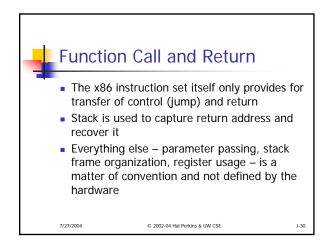


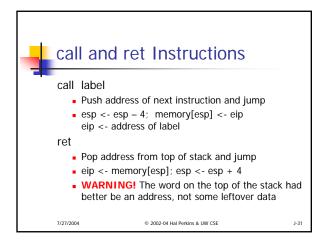
-	Conditional Jumps Following						
	mr	nemonics for i	; jump if result == 0 ; jump if result != 0 ; jump if result > 0 ; jump if result <= 0 ; jump if result >= 0 ; jump if result < 0 ; jump if result <= 0 ; jump if result >= 0 ; jump if result > 0 ssembler is providing multiple opcode ndividual instructions , it will probably be the result of an optimi	mization			
	7/27/2004	l	© 2002-04 Hal Perkins & UW CSE	J-26			

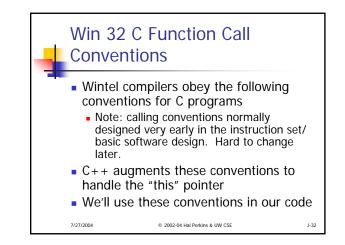


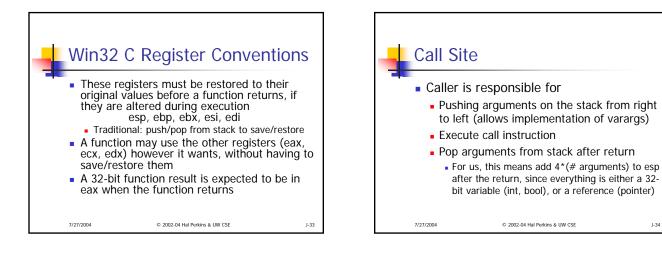


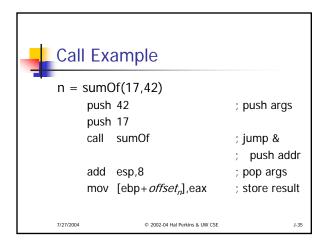


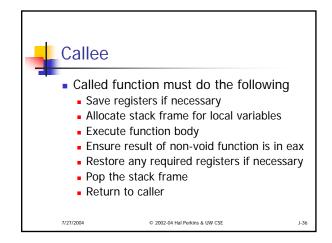












J-34

