#### CSEP567: Design and Implementation of Digital Systems

- Course staff:
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- Course web:
  - http://www.cs.washington.edu/education/courses/csep567/04sp/
  - My office: CSE 464 Allen Center, 206 543-6274
- Today
  - Class administration, overview of course web, and logistics
  - What is logic design?
  - What is digital hardware?
  - What will we be doing in this class?

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#### Highlights:

- -- we'll be reading hand-outs and papers from various sources.
- -- The course work will be built around an embedded-core processor in an FPGA.
- -- Tools are Active-HDL from Aldec, Synplify, and Xilinx ISE.
  - -- Languages are verilog and C.
- -- Applications in the FPGA will include some audio.
- -- Lecture-discussion for an hour or so, then into the lab for the rest of the evening.
  - -- No hardware experience required.

#### Labs:

- Lab 1- Atmel AVR Microprocessor PWM experiment
- Lab 2 Tutorials:
  - 1. Introduction to Active-HAL
  - 2. Using Verilog with Active-HDL
- Lab 3- AFX XC1000 Blink program in Verilog
- Lab 4- MicroBlaze Blink Program
- Lab 5- MicroBlaze PWM Program
- Lab 6- Verilog String Synthesis Example
- Lab 7- MicroBlaze String Controller

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#### Why are we here?

- Obvious reasons
  - this course is part of the PMP requirements
  - it is the implementation basis for all modern computing devices
    - building large things from small components
    - provide a model of how a computer works
- More important reasons
  - the inherent parallelism in hardware is often our first exposure to parallel computation
  - it offers an interesting counterpoint to software design and is therefore useful in furthering our understanding of computation, in general

#### What will we learn in CSEP567?

- The language of logic design
  - Boolean algebra, logic minimization, state, timing, CAD tools
- The concept of state in digital systems
  - analogous to variables and program counters in software systems
- How to specify/simulate/compile/realize our designs
  - hardware description languages
  - tools to simulate the workings of our designs
  - logic compilers to synthesize the hardware blocks of our designs
  - Use of IP (software microprocessor core)
- Contrast with software design
  - sequential and parallel implementations
  - specify algorithm as well as computing/storage resources it will use

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#### Applications of logic design

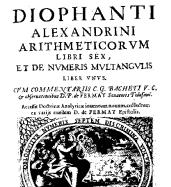
- Conventional computer design
  - CPUs, busses, peripherals
- Networking and communications
  - phones, modems, routers
- Embedded products
  - in cars, toys, appliances, entertainment devices
- Scientific equipment
  - testing, sensing, reporting
- The world of computing is much much bigger than just PCs!

# The Digital Age

- Computing is in its infancy
  - Processing power
    - Doubles every 18 months
    - Factor of 100 / decade
  - Disk capacity
    - Doubles every 12 months
    - Factor of 1000 / decade
  - Optical fiber transmission capacity
    - Doubles every 9 months
    - Factor of 10,000 / decade
- The bases are mathematics and switches
  - How did we get here?

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#### Diophantus of Alexandria b. ~200 BCE



Known as the "father of algebra"

Arithmetica is a collection of 130 problems that gives numerical solutions of determinate equations, which have a unique solution, and indeterminate equations.

The Later Alexandrian Age was a time when mathematicians were discovering many ideas that lead to our concept of mathematics today.

#### 850 AD



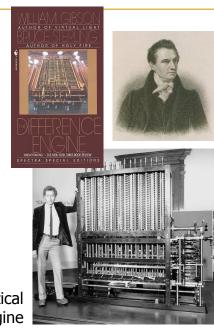
- Abu Ja'far Muhammad ibn Musa al-Khwarizmi
- Lived in Baghdad, 780 to 850 AD.
   One of the first to write on algebra (using words, not letters) and also Hindu-Arabic numbers (1, 2, 3, ...).
- From his name and writings came the words "algebra" and "algorithm".
- Book: Hisab al-jabr w'al-muqabala

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#### 1822

- Charles Babbage
  - Father of computing
- 1822 Difference Engine
  - A calculator
- 1834 Analytical Engine
  - A computer
  - Programmable



Analytical Engine

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#### 1854

- George Boole
  - Boolean algebra
- Number system with 2 values
  - □ 0/1 ⇔ false/true
  - Do math on logic statements
  - □ 3 operations (NOT, AND, OR)

	No.	
4	2	

All computers use Boolean algebra

NOT						
A Out						
0	1					
1 0						

AND					
Α	В	Out			
0	0	0			
0	1	0			
1	0	0			
1	1	1			

OR							
A B Out							
0	0	0					
0	1	1					
1	0	1					
1	1	1					

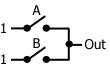
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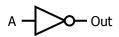
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#### 1938

- Claude Shannon
  - Implemented Boolean algebra using switches
  - Described information using binary digits (bits)







Α	Out
0	1
1	0

**NOT** 

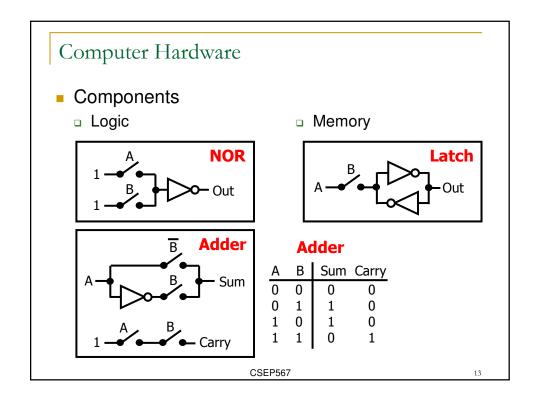
Α	, B	
1 —	••	Out

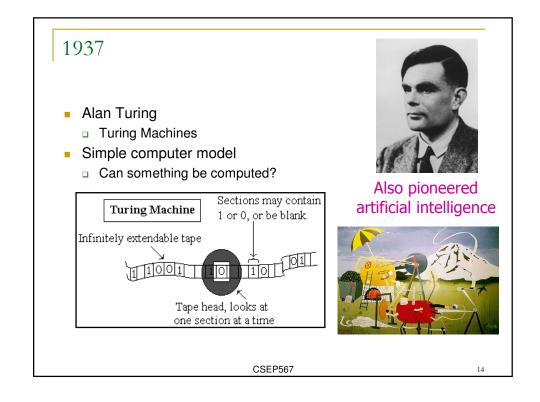
AND					
Α	В	Out			
0	0	0			
0	1	0			
1	0	0			
1	1	1			

0	R

Α	В	Out
0	0	0
0	1	1
1	0	1
1	1	1

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# 1945

- John von Neumann
  - □ First stored computer program
- A sequence of operations
  - Read from memory
  - Operate using logic gates
  - Store result into memory



Other contributions: Quantum Mechanics Cellular Automata Game Theory

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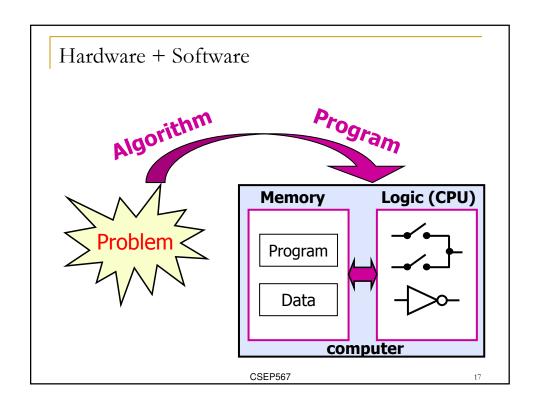
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# Stored Programs = Software



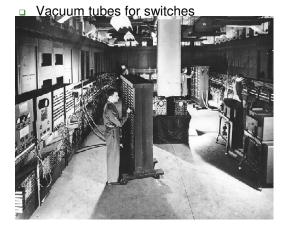
Bill Gates and Paul Allen, Lakeside, 1968

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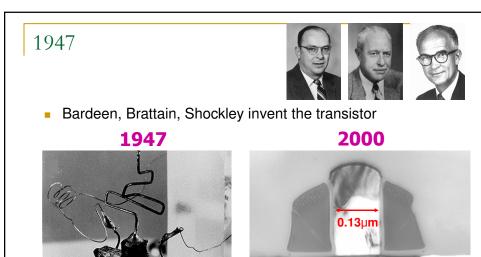


■ ENIAC...the first computer

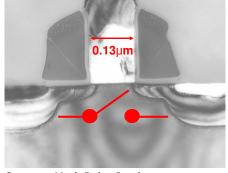


1000x faster than anything before... 19,000 tubes 200 kilowatts 357 multiplies per second

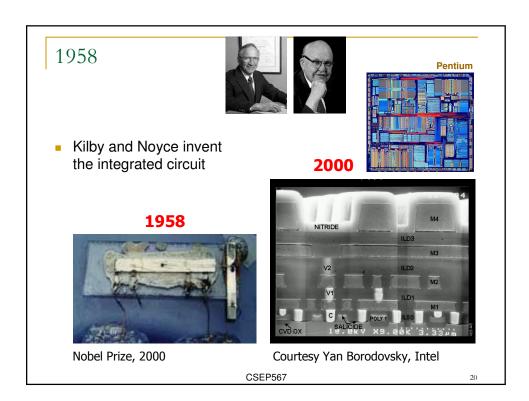
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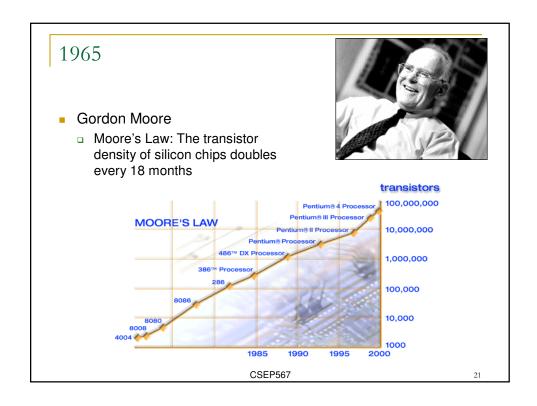


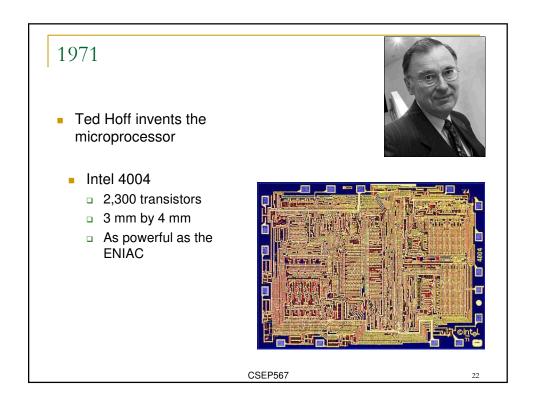
Nobel Prize, 1956

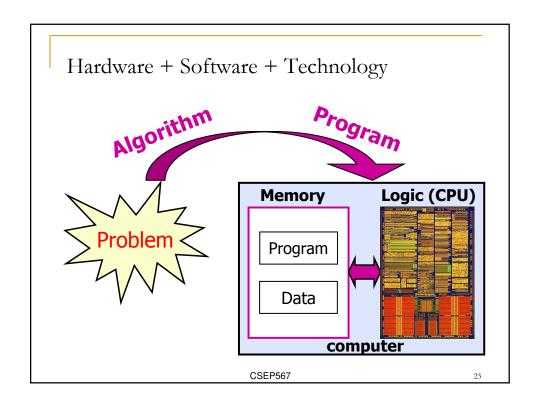


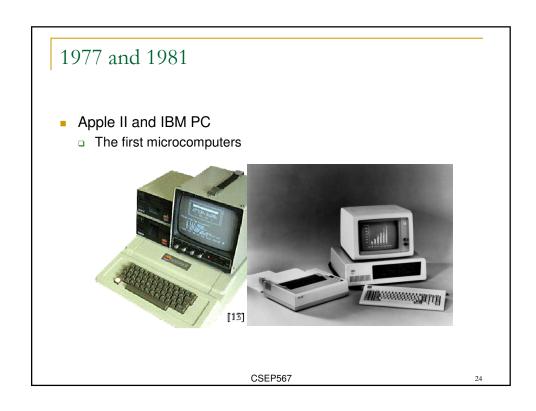
Courtesy Mark Bohr, Intel CSEP567

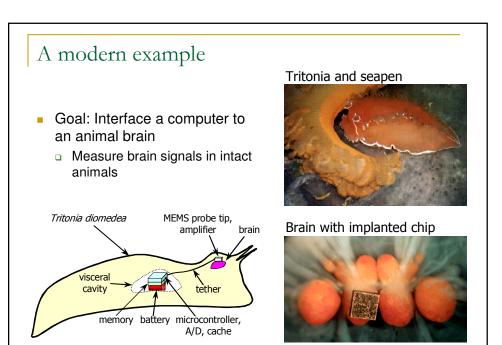






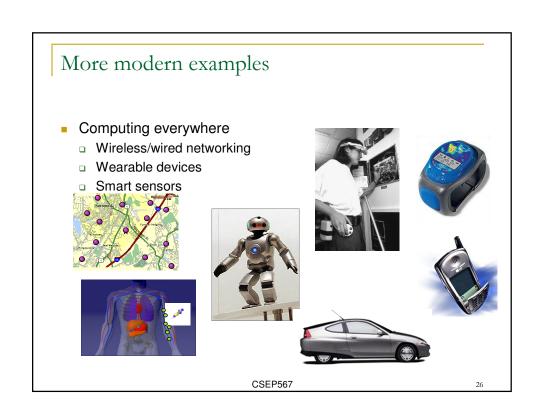






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Courtesy Jim Beck and Russell Wyeth



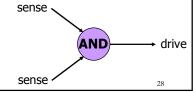
#### What is logic design?

- What is design?
  - given a specification of a problem, come up with a way of solving it choosing appropriately from a collection of available components
  - while meeting some criteria for size, cost, power, beauty, elegance, etc.
- What is logic design?
  - determining the collection of digital logic components to perform a specified control and/or data manipulation and/or communication function and the interconnections between them
  - which logic components to choose? there are many implementation technologies (e.g., off-the-shelf fixed-function components, programmable devices, transistors on a chip, etc.)
  - the design may need to be optimized and/or transformed to meet design constraints

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# What is digital hardware?

- Collection of devices that sense and/or control wires that carry a digital value (i.e., a physical quantity that can be interpreted as a "0" or "1")
  - example: digital logic where voltage < 0.8v is a "0" and > 2.0v is a "1"
  - example: pair of transmission wires where a "0" or "1" is distinguished by which wire has a higher voltage (differential)
  - example: orientation of magnetization signifies a "0" or a "1"
- Primitive digital hardware devices
  - logic computation devices (sense and drive)
    - are two wires both "1" make another be "1" (AND)
    - is at least one of two wires "1" make another be "1" (OR)
    - is a wire "1" then make another be "0" (NOT)
  - memory devices (store)
    - store a value
    - recall a previously stored value



#### What is happening now in digital design?

- Important trends in how industry does hardware design
  - larger and larger designs
  - shorter and shorter time to market
  - cheaper and cheaper products
- Scale
  - pervasive use of computer-aided design tools over hand methods
  - multiple levels of design representation
- Time
  - emphasis on abstract design representations
  - programmable rather than fixed function components
  - automatic synthesis techniques
  - importance of sound design methodologies
- Cost
  - higher levels of integration
  - use of simulation to debug designs
  - simulate and verify before you build

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# Computation: abstract vs. implementation

- Up to now, computation has been a mental exercise (paper, programs)
- This class is about physically implementing computation using physical devices that use voltages to represent logical values
- Basic units of computation are:

```
representation: "0", "1" on a wire
```

set of wires (e.g., for binary ints)

□ assignment: x = y□ data operations: x + y - 5

control:

sequential statements: A; B; C

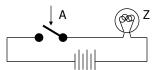
conditionals: if x == 1 then y loops: for (i = 1; i == 10, i++)

procedures: A; proc(...); B;

 We will study how each of these are implemented in hardware and composed into computational structures

# Switches: basic element of physical implementations

Implementing a simple circuit (arrow shows action if wire changes to "1"):



close switch (if A is "1" or asserted) and turn on light bulb (Z)



open switch (if A is "0" or unasserted) and turn off light bulb (Z)

$$Z \equiv A$$

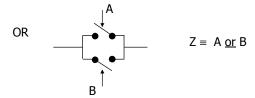
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# Switches (cont'd)

Compose switches into more complex ones (Boolean functions):

AND 
$$Z \equiv A \text{ and } B$$



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# Switching networks

- Switch settings
  - determine whether or not a conducting path exists to light the light bulb
- To build larger computations
  - use a light bulb (output of the network) to set other switches (inputs to another network).
- Connect together switching networks
  - to construct larger switching networks, i.e., there is a way to connect outputs of one network to the inputs of the next.

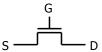
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#### Transistor networks

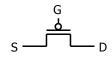
- Modern digital systems are designed in CMOS technology
  - MOS stands for Metal-Oxide on Semiconductor
  - C is for complementary because there are both normally-open and normally-closed switches
- MOS transistors act as voltage-controlled switches
  - similar, though easier to work with than relays.

#### MOS transistors

- MOS transistors have three terminals: drain, gate, and source
  - they act as switches in the following way:
     if the voltage on the gate terminal is (some amount) higher/lower
     than the source terminal then a conducting path will be
     established between the drain and source terminals



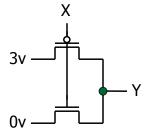
n-channel open when voltage at G is low closes when: voltage(G) > voltage (S) + ε



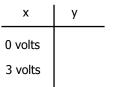
p-channel closed when voltage at G is low opens when: voltage(G) < voltage (S)  $-\epsilon$ 

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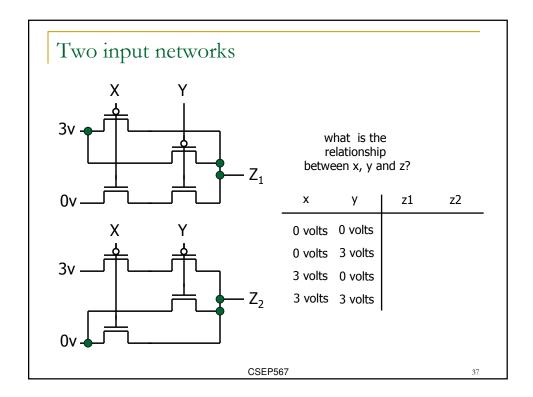
#### MOS networks



what is the relationship between x and y?



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# Speed of MOS networks

- What influences the speed of CMOS networks?
  - charging and discharging of voltages on wires and gates of transistors
- Capacitors hold charge
  - capacitance is at gates of transistors and wire material
- Resistors slow movement of electrons
  - resistance mostly due to transistors

# Representation of digital designs

- Physical devices (transistors, relays)
- Switches
- Truth tables
- Boolean algebra
- Gates
- Waveforms
- Finite state behavior
- Register-transfer behavior.
- Concurrent abstract specifications

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scope of CSE P 567

#### Digital vs. analog

- Convenient to think of digital systems as having only discrete, digital, input/output values
- In reality, real electronic components exhibit continuous, analog, behavior
- Why do we make the digital abstraction anyway?
  - switches operate this way
  - easier to think about a small number of discrete values
- Why does it work?
  - does not propagate small errors in values
  - always resets to 0 or 1

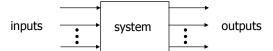
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# Mapping from physical world to binary world

Technology	State 0	State 1	
Relay logic CMOS logic Transistor transistor logic (TTL) Fiber Optics Dynamic RAM Nonvolatile memory (erasable) Programmable ROM Bubble memory Magnetic disk Compact disc	Circuit Open 0.0-1.0 volts 0.0-0.8 volts Light off Discharged capacitor Trapped electrons Fuse blown No magnetic bubble No flux reversal No pit	Circuit Closed 2.0-3.0 volts 2.0-5.0 volts Light on Charged capacitor No trapped electrons Fuse intact Bubble present Flux reversal Pit	
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# Combinational vs. sequential digital circuits

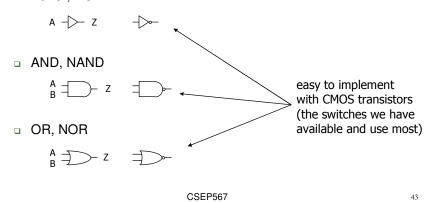
A simple model of a digital system is a unit with inputs and outputs:



- Combinational means "memory-less"
  - a digital circuit is combinational if its output values only depend on its input values

#### Combinational logic symbols

- Common combinational logic systems have standard symbols called logic gates
  - Buffer, NOT



#### Sequential logic

- Sequential systems
  - exhibit behaviors (output values) that depend not only on the current input values, but also on previous input values
- In reality, all real circuits are sequential
  - because the outputs do not change instantaneously after an input change
  - why not, and why is it then sequential?
- A fundamental abstraction of digital design is to reason (mostly) about steady-state behaviors
  - look at the outputs only after sufficient time has elapsed for the system to make its required changes and settle down

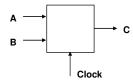
# Synchronous sequential digital systems

- Outputs of a combinational circuit depend only on current inputs
  - after sufficient time has elapsed
- Sequential circuits have memory
  - even after waiting for the transient activity to finish
- The steady-state abstraction is so useful that most designers use a form of it when constructing sequential circuits:
  - the memory of a system is represented as its state
  - changes in system state are only allowed to occur at specific times controlled by an external periodic clock
  - the clock period is the time that elapses between state changes it must be sufficiently long so that the system reaches a steady-state before the next state change at the end of the period

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#### Example of combinational and sequential logic

- Combinational:
  - input A, B
  - wait for clock edge
  - observe C
  - wait for another clock edge
  - observe C again: will stay the same
- Sequential:
  - input A, B
  - wait for clock edge
  - observe C
  - wait for another clock edge
  - observe C again: may be different



#### Abstractions

- Some we've seen already
  - digital interpretation of analog values
  - transistors as switches
  - switches as logic gates
  - use of a clock to realize a synchronous sequential circuit
- Some others we will see
  - truth tables and Boolean algebra to represent combinational logic
  - encoding of signals with more than two logical values into binary form
  - state diagrams to represent sequential logic
  - hardware description languages to represent digital logic
  - waveforms to represent temporal behavior

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#### An example

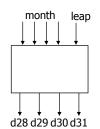
- Calendar subsystem: number of days in a month (to control watch display)
  - used in controlling the display of a wrist-watch LCD screen
  - inputs: month, leap year flag
  - outputs: number of days

# Implementation in software

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# Implementation as a combinational digital system

- Encoding:
  - how many bits for each input/output?
  - binary number for month
  - four wires for 28, 29, 30, and 31
- Behavior:
  - combinational
  - truth table specification



month	leap	d28	d29	<u>d30</u>	<u>d3:</u>
0000	- '	_	-	-	_
0001	-	0	0	0	1
0010	0	1	0	0	0
0010	1	0	1	0	0
0011	_	0	0	0	1
0100	_	0	0	1	0
0101	_	0	0	0	1
0110	_	0	0	1	0
0111	_	0	0	0	1
1000	_	0	0	0	1
1001	_	0	0	1	0
1010	_	0	0	0	1
1011	_	0	0	1	0
1100	_	0	0	0	1
1101	_	-	_	-	_
111-	_	-	_	-	_
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#### Combinational example (cont'd)

```
Truth-table to logic to switches to gates
```

```
symbol
\Box d28 = 1 when month=0010 and leap=0
                                                   for <u>not</u>
d28 = m8'•m4'•m2•m1'•leap'
```

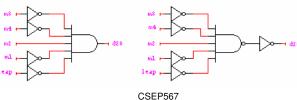
- □ d31 = 1 when month=0001 or month=0011 or ... month=1100
- $d31 = (m8' \cdot m4' \cdot m2' \cdot m1) + (m8' \cdot m4' \cdot m2 \cdot m1) + ...$ (m8•m4•m2'•m1') /

```
month
0001
                                                             d28 d29 d30 d31
                                                      leap
□ d31 = can we simplify more?
                                                      0
                                            0010
                                                                       0
                                                                            0
                                            0010
                                                      1
                                                                       0
                                                                            0
                               symbol
                symbol
for <u>and</u>
                                            0011
                                for or
                                            0100
                                            1100
                                            1101
                                            111-
                                            0000
```

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#### Combinational example (cont'd)

- d28 = m8'•m4'•m2•m1'•leap'
- d29 = m8'•m4'•m2•m1'•leap
- $d30 = (m8' \cdot m4 \cdot m2' \cdot m1') + (m8' \cdot m4 \cdot m2 \cdot m1') +$  $(m8 \cdot m4' \cdot m2' \cdot m1) + (m8 \cdot m4' \cdot m2 \cdot m1)$ 
  - $= (m8' \cdot m4 \cdot m1') + (m8 \cdot m4' \cdot m1)$
- $d31 = (m8' \cdot m4' \cdot m2' \cdot m1) + (m8' \cdot m4' \cdot m2 \cdot m1) +$  $(m8' \cdot m4 \cdot m2' \cdot m1) + (m8' \cdot m4 \cdot m2 \cdot m1) +$  $(m8 \cdot m4' \cdot m2' \cdot m1') + (m8 \cdot m4' \cdot m2 \cdot m1') +$ (m8•m4•m2'•m1')



# Activity

How much can we simplify d31?

 What if we started the months with 0 instead of 1? (i.e., January is 0000 and December is 1011)

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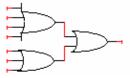
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#### Combinational example (cont'd)

```
d28 = m8'•m4'•m2•m1'•leap'
```

- d29 = m8'•m4'•m2•m1'•leap
- $d30 = (m8' \cdot m4 \cdot m2' \cdot m1') + (m8' \cdot m4 \cdot m2 \cdot m1') + (m8 \cdot m4' \cdot m2' \cdot m1) + (m8 \cdot m4' \cdot m2 \cdot m1)$





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# Another example

- Door combination lock:
  - punch in 3 values in sequence and the door opens; if there is an error the lock must be reset; once the door opens the lock must be reset
  - inputs: sequence of input values, reset
  - outputs: door open/close
  - memory: must remember combination or always have it available as an input

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#### Implementation in software

```
integer combination_lock ( ) {
   integer v1, v2, v3;
   integer error = 0;
   static integer c[3] = 3, 4, 2;

   while (!new_value( ));
   v1 = read_value( );
   if (v1 != c[1]) then error = 1;

   while (!new_value( ));
   v2 = read_value( );
   if (v2 != c[2]) then error = 1;

   while (!new_value( ));
   v3 = read_value( );
   if (v2 != c[3]) then error = 1;

   if (v2 != c[3]) then error = 1;

   if (error == 1) then return(0); else return (1);
}
```

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# Implementation as a sequential digital system

- Encoding:
  - how many bits per input value?
  - how many values in sequence?
  - how do we know a new input value is entered?
  - how do we represent the states of the system?
- Behavior:
  - clock wire tells us when it's ok to look at inputs
     (i.e., they have settled after change)
  - sequential: sequence of values must be entered
  - sequential: remember if an error occurred
  - finite-state specification

new value reset

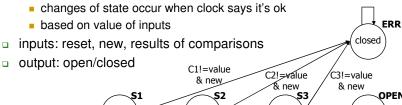
clock state

d open/closed

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# Sequential example (cont'd): abstract control

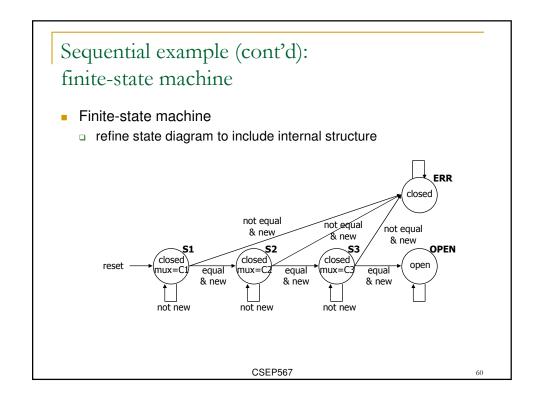
- Finite-state diagram
  - states: 5 states
    - represent point in execution of machine
    - each state has outputs
  - transitions: 6 from state to state, 5 self transitions, 1 global



reset Closed C1=value Closed C2=value C3=value Open Open Open Not new Not new

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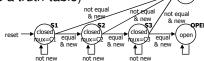
#### Sequential example (cont'd): data-path vs. control Internal structure data-path control finite-state machine controller storage for combination comparators control for data-path state changes controlled by clock new equal reset value mux multiplexer controller control clock comparator equal open/closed



# Sequential example (cont'd): finite-state machine

#### Finite-state machine

generate state table (much like a truth-table)



				next		not new	1100 11011	not new
reset	new	equal	state	state	mux	open/closed	_	
1	-	-	-	S1	C1	closed		
0	0	-	S1	S1	C1	closed		
0	1	0	S1	ERR	_	closed		
0	1	1	S1	S2	C2	closed		
0	0	_	S2	S2	C2	closed		
0	1	0	S2	ERR	-	closed		
0	1	1	S2	S3	C3	closed		
0	0	-	S3	S3	C3	closed		
0	1	0	S3	ERR	-	closed		
0	1	1	S3	OPEN	_	open		
0	_	_	OPEN	OPEN	_	open		
0	-	-	ERR	ERR	-	closed		

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# Sequential example (cont'd): encoding

#### Encode state table

- state can be: S1, S2, S3, OPEN, or ERR
  - needs at least 3 bits to encode: 000, 001, 010, 011, 100
  - and as many as 5: 00001, 00010, 00100, 01000, 10000
  - choose 4 bits: 0001, 0010, 0100, 1000, 0000
- output mux can be: C1, C2, or C3
  - needs 2 to 3 bits to encode
  - choose 3 bits: 001, 010, 100
- output open/closed can be: open or closed
  - needs 1 or 2 bits to encode
  - choose 1 bits: 1, 0

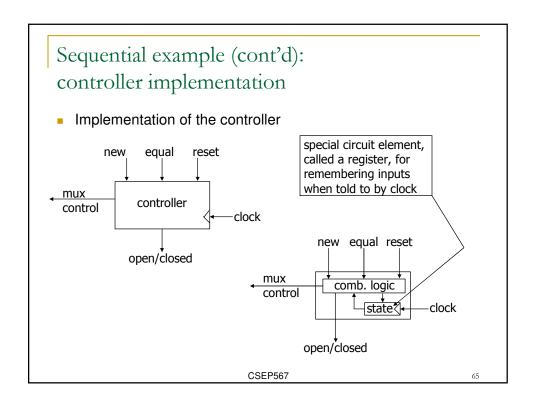
# Sequential example (cont'd): encoding

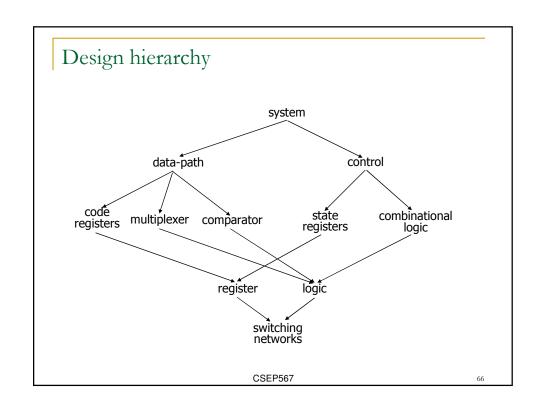
- Encode state table
  - □ state can be: S1, S2, S3, OPEN, or ERR
    - choose 4 bits: 0001, 0010, 0100, 1000, 0000
  - output mux can be: C1, C2, or C3
    - choose 3 bits: 001, 010, 100
  - output open/closed can be: open or closed
    - choose 1 bits: 1, 0

					next			
	reset	new	equal	state	state	mux	open/	<u>closed</u>
	1	_	- '	-	0001	001	0	
	0	0	-	0001	0001	001	0	
	0	1	0	0001	0000	-	0	good choice of encoding!
	0	1	1	0001	0010	010	0	
	0	0	-	0010	0010	010	0	mux is identical to last 3 bits of state
	0	1	0	0010	0000	-	0	
	0	1	1	0010	0100	100	0	last 3 bits of state
	0	0	-	0100	0100	100	0	open/closed is identical to first bit of state
	0	1	0	0100	0000	-	0	
	0	1	1	0100	1000	-	1	
	0	-	-	1000	1000	-	1	or state
	0	-	-	0000	0000	-	0	
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# Activity

 Have lock always wait for 3 key presses exactly before making a decision





#### Summary

- That was what the entire course is about (mostly)
  - converting solutions to problems into combinational and sequential networks effectively organizing the design hierarchically
  - doing so with a modern set of design tools that lets us handle large designs effectively
  - taking advantage of optimization opportunities
  - Exploring pre-packaged IP (cores)
- Now lets do it again
  - this time we'll take nine weeks instead of one