

Research Interests

Reconfigurable and low-power architecture. EDA algorithms.

Accomplishments

- Successfully completed the following projects:
 - Researching and developing new CAD routing algorithm enhancements.
 - Developing real-time fluid simulator for high-frequency, parallel hardware in Verilog.
 - Creating wireless sensor network on the 8-bit Berkeley Mote platform in TinyOS.
 - Laying out and verifying VLSI CMOS design with self-developed standard-cell library using Synopsys, Cadence, and HSpice tools.
 - Designed and constructed analog capacitance meter and low-noise biopotential amplifier.
- Won, as an undergraduate, *FPGA Technology Best Paper Award* for research on novel EDA routing technique at Field Programmable Logic Conference.
- Showed ability to properly scope, document, and deliver a product by designing, implementing, and demonstrating large, team hardware project.
- Demonstrated leadership skills by leading and training teams of 10 to 25 young people as part of full-time volunteer work from 2002 to 2004.

Education

Ph.D. Computer Engineering, Anticipated 2011.
University of Washington, Seattle, WA.

B.S. Computer Engineering, *Magna Cum Laude*. August 2006. **3.9** GPA.
Brigham Young University, Provo, UT

Relevant Experience

Research Assistant **Jan '06 – Present**
University of Washington, Computer Science and Engineering Dept., Seattle, WA
Researched coarse-grained reconfigurable architectures and pipelined EDA algorithms.
Implemented architecture exploration tools in Java. Published architecture and algorithms.

Architecture Research Intern **Jun '07 – Sep '07**
Microsoft Research, Hardware Devices Group. Redmond, WA
Researched CAM based reconfigurable architecture. Implemented large CAMs in Verilog.

Software Engineer Intern **May '05 – Aug '05**
Tabula Inc., EDA Router Tools, Santa Clara, CA
Designed, developed, and tested custom EDA routing algorithms, in C++ and Verilog, for programmable architecture. Researched and invented routing algorithm improvements.

Teaching Assistant **Jan '05 – Apr '05**
Brigham Young University, Electrical Engineering Dept., Provo, UT
Taught advanced circuit design lab and assisted students in completing labs using standard lab equipment. Assisted with circuit verification by hand analysis, MATLAB, and PSpice.

Publications

Allan Carroll and Carl Ebeling. "Reducing The Space Complexity Of Pipelined Routing Using Modified Range Encoding," In *Intl. Conference on Field Programmable Logic and Applications* (FPL 2006), pp. 613-618. Madrid, Spain, September, 2006 (Award Paper).