# SYNTHESIS OF MULTIPLE-INPUT TRANSLINEAR ELEMENT NETWORKS

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**ABSTRACT**

*We describe two systematic procedures for synthesizing* mutliple-input translinear element *(MITE) networks that produce an output current that is equal to product of a number of input currents, each of which is raised to an arbitrary rational power. By using the first procedure, we obtain a MITE network, called a* two-layer network, *that is relatively insensitive to mismatch in the MITE weight values. By using the second procedure, we arrive at a MITE network, called a* cascade network, *that reduces the fan-in required of each MITE. We illustrate each of these procedures with an example.*

## 1. MITE NETWORKS: THE SYNTHESIS PROBLEM

We recently introduced a class of translinear circuits, called *multiple-input translinear element* (MITE) *networks*, that accurately embody product-of-power-law relationships in the current signal domain [1–3]. The MITE is a circuit primitive that produces an output current that is exponential in a weighted sum of the MITE's input voltages [2, 4]. For a given product-of-power-law relationship, MITE networks often require fewer transistors than would translinear-loop circuits [5, 6]. In some cases, MITE networks can operate on a lower power-supply voltage than could corresponding translinear-loop circuits. Here, we describe two systematic procedures for synthesizing MITE networks to implement any given product-of-power-law relationship between a single output and any number of input currents for which the power-laws are rational numbers. Using the first of these procedures, we obtain a MITE network, called a *two-layer network*, that is relatively insensitive to mismatch in the MITE weight values. Using the second procedure, we obtain a MITE network, called a *cascade network*, that reduces the fan-in required for each MITE.

We now define the scope of the synthesis problem that we shall consider in this paper. Suppose that we are given an expression relating a single output current, $I_{N+1}$, to $N$ input currents, $I_1$ through $I_N$, of the form

$$I_{N+1} = \prod_{n=1}^{N} I_n^{\Lambda_n}, \tag{1}$$

where $\Lambda_1$ through $\Lambda_N$ are dimensionless rational numbers (either positive or negative). In order for the units of Eq. 1 to balance properly, we must have that

$$\sum_{n=1}^{N} \Lambda_n = 1.$$

Our objective in solving the synthesis problem will be to construct a MITE network that embodies Eq. 1, given $\Lambda_1$ through $\Lambda_N$.

Because we have restricted the values of $\Lambda_1$ through $\Lambda_N$ to the rational numbers, we have that

$$|\Lambda_n| = \frac{p_n}{q_n},$$

where $p_n$ and $q_n$ are integers for each $n$. Further, we assume that, for each $n$, $p_n$ and $q_n$ have no common divisors other than unity. Without loss of generality, we will also assume that $\Lambda_1$ through $\Lambda_J$ are positive and that $\Lambda_{J+1}$ through $\Lambda_N$ are negative, so $I_{N+1}$ is of the form

$$I_{N+1} = \frac{\prod_{n=1}^{J} I_n^{\Lambda_n}}{\prod_{n=J+1}^{N} I_n^{|\Lambda_n|}}.$$

We can always renumber the input currents so that the expression to be implemented with a MITE network is in this form.

We could consider the case of simultaneously implementing a number of different product-of-power-law relationships of the form of Eq. 1 holding among overlapping sets of input currents. In considering multiple expressions simultaneously, we can often share input MITEs corresponding to the common inputs currents. In so doing, we would not have to supply multiple copies of these inputs, as we would if we implemented each expression with an independent circuit. Sometimes, we can see where hardware can be shared between several single-output circuits. However, systematic synthesis procedures applicable to the multiple-output case are difficult to formulate and to state succinctly; such cases can be handled by formulating the synthesis of MITE networks as a constrained optimization problem [2].

Seevinck has described various aspects of the systematic synthesis of translinear circuits [6]. He adopts a higher-level view of the synthesis problem than we do in this paper. He begins with a mathematical function of a dimensionless variable to be realized with translinear-loop circuits. He discusses various techniques for decomposing into and approximating these functions by forms suitable for realization with translinear circuits. We can use all of Seevinck's techniques directly with the synthesis procedures that we describe in this paper to implement analog signal-processing functions with MITE networks in place of translinear circuits.

## 2. SYNTHESIS OF MITE NETWORKS

Like many circuit synthesis problems, the problem of synthesizing MITE networks is underconstrained—the given information (e.g., the values of $\Lambda_1$ through $\Lambda_N$) does not uniquely determine the form of the circuit (e.g., the MITE network) to be synthesized. We have shown that, if there exists a single MITE network implementing an expression of the form of Eq. 1, then there exists a countable infinity of such MITE networks [2]. Given this fact, by what criteria are we to choose one from among them? In order that the power-law relationships embodied in our MITE networks be independent of parasitics and device parameters, we require that each MITE has the same complement of inputs [2]. Consequently, other considerations aside, it seems as though we would prefer a MITE network that uses fewer inputs per MITE.



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In general, however, we must consider other criteria to make this choice. For example, we could consider the sensitivity of different MITE network topologies to component mismatch. In Section 2.1, we show that Eq. 1 can be implemented in a MITE network with a *two-layer* structure. The first layer, called the *numerator layer*, feeds directly into the output MITE and comprises all of the input MITEs whose currents are raised to positive powers. The second layer, called the *denominator layer*, feeds into the numerator layer and comprises all of the input MITEs whose currents are raised to negative powers. All of the paths in a two-layer network are as short as possible, so component mismatch will not accumulate over long cascades. However, if there are a large number of currents raised to positive powers, then there will be a large number of inputs converging on the output MITE. In this case, we will have to use a large number of inputs for the output MITE, and hence for every MITE.

In Section 2.2, we show that Eq. 1 can be implemented in a MITE network with a *cascade* structure. In this case, we arrange the input MITEs into a linear sequence, alternating between those MITEs whose currents appear in the numerator of the expression implemented by the MITE network and those whose currents appear in the denominator of the expression. In this case, each MITE will have some self connections and inputs the next MITE in the sequence. Consequently, for a given expression, a cascade network will generally have a fewer inputs per MITE than would a two-layer network. However, because the average path length between input and output is longer in a cascade network than it is in a two-layer network, we expect that a cascade network will be more sensitive to component mismatch than would be an equivalent two-layer network.

### *2.1 Construction of a Two-Layer MITE Network*

We begin the construction of a two-layer MITE network embodying Eq. 1 by creating a MITE for the output current and labeling it $Q_{N+1}$. The remainder of the procedure is as follows:

1. *Constructing the numerator layer*: For each value of $n$ between 1 and $J$, we perform the following steps. First, we create a MITE for the $n$th input current, labeling it $Q_n$. Then, we diode connect MITE $Q_n$ through $q_n$ unit weights, and we connect MITE $Q_n$ to MITE $Q_{N+1}$ through $p_n$ unit weights.
2. *Constructing the denominator layer*: For each value of $n$ between $J$+1 and $N$, we perform the following steps. First, we create a MITE for the $n$th input current, labeling it $Q_n$. Then, we pick one of the MITEs in the numerator layer—say MITE $Q_m$. Let $k$ denote the greatest common divisor (g.c.d.) of $p_m q_n$ and $p_n q_m$. Then, we diode connect MITE $Q_n$ through $p_m q_n / k$ unit weights and we connect MITE $Q_n$ to MITE $Q_m$ through $p_n q_m / k$ unit weights.
3. *Adding the required number of unused inputs*: We denote by $K$ the largest number of inputs feeding into any MITE. If each MITE happens to have $K$ inputs, we are done. Otherwise, we add a sufficient number of grounded unit weights to each MITE that they each have $K$ inputs.

### *2.2 Construction of a Cascade MITE Network*

We begin the construction of a cascade MITE network implementing Eq. 1 by creating a MITE for the output current, labeling it $Q_{N+1}$. The remainder of the procedure is as follows:

1. We begin with an input current from the numerator of Eq. 1—say the $n$th input current—and we create a MITE for it, labeling it $Q_n$. We diode connect MITE $Q_n$ through $q_n$ unit weights, and we connect MITE $Q_n$ to MITE $Q_{N+1}$ through $p_n$ unit weights.
2. We choose an input current from the denominator of Eq. 1. If there are none left, then we proceed to step 5. Otherwise, if we chose the $n$th input current, we create a MITE for it, labeling it $Q_n$. Suppose that the MITE created in the previous step was MITE $Q_m$. Let $k$ denote the g.c.d. of $p_m q_n$ and $p_n q_m$. Then, we diode connect MITE $Q_n$ through $p_m q_n / k$ unit weights and we connect MITE $Q_n$ to MITE $Q_m$ through $p_n q_m / k$ unit weights.
3. We choose an input current from the numerator of Eq. 1. If there are none left, then we proceed to step 6. Otherwise, if we chose the $n$th input current, we create a MITE for it, labeling it $Q_n$. Suppose that the MITE created in the previous step was MITE $Q_m$. Let $k$ denote the g.c.d. of $p_m q_n$ and $p_n q_m$. Then, we diode connect MITE $Q_n$ through $p_m q_n / k$ unit weights and we connect MITE $Q_n$ to MITE $Q_m$ through $p_n q_m / k$ unit weights.
4. We return to step 2.
5. For each of the remaining numerator input currents, we perform the following steps. For the $n$th input, we first create a new MITE, labeling it $Q_n$. We diode connect MITE $Q_n$ through $q_n$ unit weights, and we connect MITE $Q_n$ to MITE $Q_{N+1}$ through $p_n$ unit weights. Once we exhaust the numerator input currents, we proceed to step 7.
6. For each of the remaining denominator input currents, we perform the following steps. For the $n$th input, we first create a new MITE, labeling it $Q_n$. Suppose that the MITE created in step 1 was MITE $Q_m$. Let $k$ denote the g.c.d. of $p_m q_n$ and $p_n q_m$. Then, we diode connect MITE $Q_n$ through $p_m q_n / k$ unit weights and we connect MITE $Q_n$ to MITE $Q_m$ through $p_n q_m / k$ unit weights.
7. We denote by $K$ the largest number of inputs feeding into any MITE. If each MITE happens to have $K$ inputs, we are done. Otherwise, we add a sufficient number of grounded unit weights to each MITE that they each have $K$ inputs.

### *2.3 An Illustrative Example*

In this section, we shall illustrate each of the two MITE-network construction procedures described in Sections 2.1 and 2.2 by applying them in turn to generate MITE networks to implement

$$I_6 = \frac{I_1^{1/2} I_2^{3/2} I_3}{I_4^2 I_5}. \qquad (2)$$

Throughout this section, when we first consider a new input or output current, we shall add another MITE to the circuit being made, labeling it with the number of the corresponding current.

First, using the procedure described in Section 2.1, we shall construct a two-layer MITE network realizing Eq. 2. Each of the steps in this process is illustrated in Fig. 1. We begin by making a MITE for the output current, $I_6$. Then, we construct the numerator layer, as shown in Figs. 1a, 1b, and 1c. We begin with input current $I_1$. Because $I_1$ is raised to the $\frac{1}{2}$ power in Eq. 2, we diode connect MITE $Q_1$ through two unit inputs, and we connect MITE $Q_1$ to MITE $Q_6$ through one unit input, as shown in Fig. 1a. Next, we consider input current $I_2$. Because $I_2$ is raised to the $\frac{3}{2}$ power in Eq. 2, we diode connect MITE $Q_2$ through two unit inputs, and we connect MITE $Q_2$ to MITE $Q_6$ through three unit inputs, as shown in Fig. 1b. Finally, we consider input current $I_3$. Because $I_3$ is squared in Eq. 2, we diode connect MITE $Q_3$ through one unit input, and we connect MITE $Q_3$ to MITE $Q_6$ through two unit inputs.



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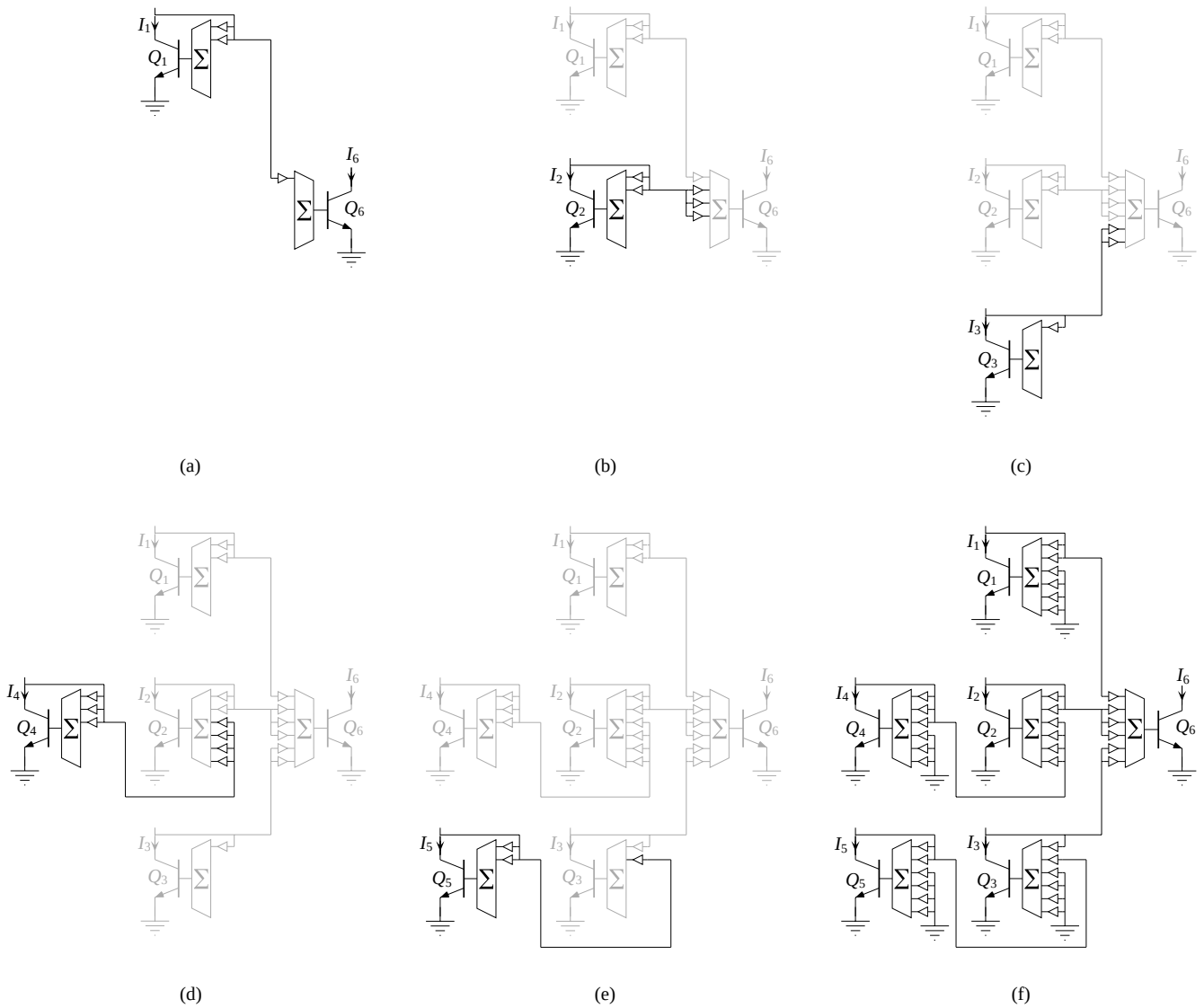


**Figure 1.** Construction of a two-layer MITE network implementing Eq. 2. We build the numerator layer in parts a, b, and c. In parts d and e, we construct the denominator layer. We add unused inputs in part f to balance the total number of unit inputs to each MITE.

Next, we construct the denominator layer, as shown in Figs. 1d and 1e. We begin with input current $I_4$. We choose to connect MITE $Q_4$ to MITE $Q_6$ through MITE $Q_2$. Because $I_2$ is raised to the $\frac{3}{2}$ power and $I_4$ is raised to the –2 power, we need to find the g.c.d. of $2\times 2=4$ and $3\times 1=3$, which is equal to 1. Then, we diode connect MITE $Q_4$ through $3\times 1/1=3$ unit inputs, and we connect MITE $Q_4$ to MITE $Q_2$ through $2\times 2/1=4$ unit inputs, as shown in Fig. 1d. Next, we consider input current $I_5$. We chose to connect MITE $Q_5$ to MITE$Q_6$ through MITE $Q_3$. Because $I_3$ is squared and $I_5$ is raised to the –1 power, we need to find the g.c.d. of $2\times 1=2$ and $1\times 1=1$, which is equal to 1. Then, we diode connect MITE $Q_5$ through $2\times 1/1=2$ unit inputs, and we connect MITE $Q_5$ to MITE $Q_3$ through $1\times 1/1=1$ unit input, as shown in Fig. 1e. Finally, we count the largest number of inputs possessed by any MITE in the circuit of Fig. 1e; this number is 6. We thus add four grounded inputs to MITEs $Q_1$, $Q_3$, and $Q_5$, and we add three grounded inputs to MITE $Q_4$, as shown in Fig. 1f. The resulting two-layer MITE network implements Eq. 2.

Using the procedure described in Section 2.2, we shall construct a cascade MITE network implementing Eq. 2. This process is illustrated in Fig. 2. Again, we begin by creating a MITE for the output current, $I_6$. We first consider input current $I_1$ from the numerator of Eq. 2. Because $I_1$ is raised to the $\frac{1}{2}$ power, we diode connect MITE $Q_1$ through two unit inputs, and we connect MITE $Q_1$ to MITE $Q_6$ through one unit input, as shown in Fig 2a. Next, we chose input current $I_5$ from the denominator of Eq. 2. Because $I_1$ is raised to the $\frac{1}{2}$ power and $I_5$ is raised to the –1 power, we need to find the g.c.d. of $1\times 1=1$ and $2\times 1=2$, which is equal to 1. So, we diode connect MITE $Q_5$ through $1\times 1/1=1$ unit input, and we connect MITE $Q_5$ to MITE $Q_1$ through $2\times 1/1=2$ unit inputs, as shown in Fig. 2b. Next, we chose input current $I_3$ from the numerator of Eq. 2. Because $I_5$ is raised to the –1 power and $I_3$ is squared, we need to find the g.c.d. of $2\times 1=2$ and $1\times 1=1$, which is equal to 1. So, we diode connect MITE $Q_3$ through $1\times 1/1=1$ unit input, and we connect MITE $Q_3$ to MITE $Q_5$ through $2\times 1/1=2$ unit inputs, as shown in Fig. 2c. Next, we chose input current $I_4$ from the denominator of Eq. 2.



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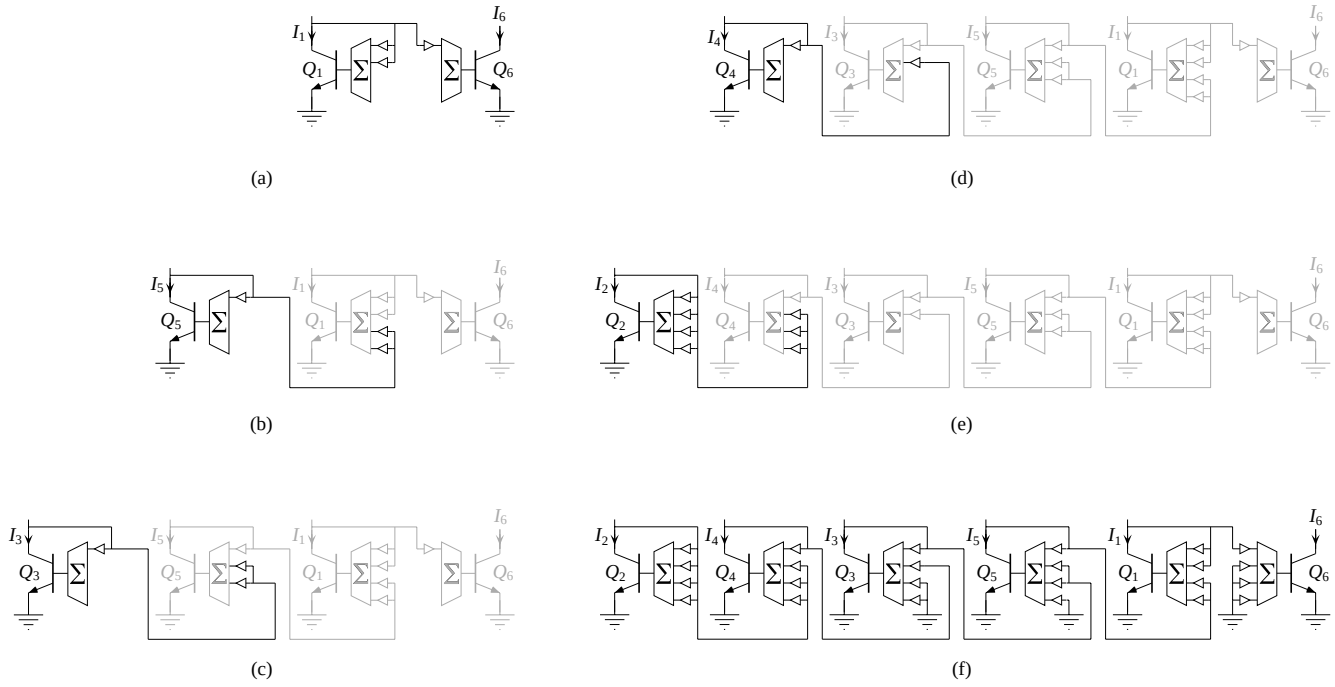


**Figure 2.** Construction of a cascade MITE network that implements Eq. 2. In part a, we begin with a current from the numerator of Eq. 2, and, in parts b, c, d, and e, we add MITEs toward the left, alternating between currents from the denominator and the numerator of Eq. 2. In part f, we add unused inputs to balance the total number of unit inputs to each MITE.

to MITE $Q_5$ through $2\times1/1=2$ unit inputs, as shown in Fig. 2c. Next, we chose input current $I_4$ from the denominator of Eq. 2. Because $I_3$ is squared and $I_4$ is raised to the –2 power, we need to find the g.c.d. of $2\times1=2$ and $2\times1=2$, which is equal to 2. So, we diode connect MITE $Q_4$ through $2\times1/2=1$ unit input, and we connect MITE$Q_4$ to MITE $Q_3$ through $2\times1/2=1$ unit input, as shown in Fig. 2d. Finally, we consider input current $I_2$ from the numerator of Eq. 2. Because $I_4$ is raised to the –2 power and $I_2$ is raised to the $\frac{3}{2}$ power, we need to find the g.c.d. of $3\times1=3$ and $2\times2=4$, which is equal to 1. So, we diode connect MITE $Q_2$ through $2\times2/1=4$ unit inputs, and we connect MITE $Q_2$ to MITE $Q_4$ through $3\times1/1=3$ unit inputs, as shown in Fig. 2e.

Finally, we count the largest number of inputs possessed by any MITE in the network of Fig. 2e; this number is 4. Consequently, we add one grounded input to MITE $Q_5$, two grounded inputs to MITE $Q_3$, and three grounded inputs to MITE $Q_6$. The resulting cascade MITE network, shown in Fig. 2f, implements Eq. 2.

## 3. CONCLUSIONS

We described two synthesis procedures by which we can construct MITE networks to implement an arbitrary product-of-power-law relationship among a single output current and any number of input currents, where the power laws are given by rational numbers. Using the first procedure, we obtain a two-layer MITE network, which minimizes the number of cascaded stages between any input and the output. Two-layer networks are thus minimally sensitive to the accumulation of mismatch in long cascades. Using the second procedure, we obtain a cascade network, which reduces the fan-in required for each MITE, but introduces long cascades between some inputs and the output, causing an accumulation of mismatch through the cascade. We illustrated each procedure using a simple example.

## 4. ACKNOWLEDGMENTS

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## 5. REFERENCES

[1] B. A. Minch, C. Diorio, P. Hasler, and C. A. Mead, "Translinear Circuits Using Subthreshold Floating-Gate MOS Transistors," *Analog Integrated Circuits and Signal Processing*, vol. 9, no. 2, pp. 167–180, 1996.

[2] B. A. Minch, *Analysis, Synthesis, and Implementation of Networks of Multiple-Input Translinear Elements*, Ph.D. Thesis, California Institute of Technology, Pasadena, CA, 1997.†

[3] B. A. Minch, P. Hasler, and C. Diorio, "Multiple-Input Translinear Element Networks," *Proceedings of the 1998 IEEE ISCAS*, Monterey, CA, vol. 1, pp. 88–91, June 1998.

[4] B. A. Minch, P. Hasler, and C. Diorio, "The Multiple-Input Translinear Element: A Versatile Circuit Element," *Proceedings of the 1998 IEEE ISCAS*, Monterey, CA, vol. 1, pp. 527–530, June 1998.

[5] B. Gilbert, "Translinear Circuits: A Proposed Classification," *Electronics Letters*, vol. 11, no. 1, pp. 14–16, 1975; and errata, vol. 11, no. 6, p. 136, 1975.

[6] E. Seevinck, *Analysis and Synthesis of Translinear Integrated Circuits*, Amsterdam, The Netherlands: Elsevier, 1988.

†Available at http://www.ee.cornell.edu/~minch/thesis.html.



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