

Multiple-Input Translinear Element Networks

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Abstract—We describe a new class of translinear circuits that accurately embody product-of-power-law relationships in the current signal domain. We call such circuits multiple-input translinear element (MITE) networks. A MITE is a circuit element, which we defined recently, that produces an output current that is exponential in a weighted sum of its input voltages. We describe intuitively the basic operation of MITE networks and provide a systematic matrix technique for analyzing the nonlinear relationships implemented by any given circuit. We also show experimental data from three MITE networks that were fabricated in a 1.2- μm double-poly CMOS process.

Index Terms—Current-mode circuits, floating-gate circuits, nonlinear circuits, translinear circuits.

I. PRODUCT-OF-POWER-LAW CIRCUITS

PRODUCTS, quotients, and power-law relationships figure prominently in many signal- and information-processing algorithms. Consequently, analog circuits embodying such relationships are important components in the construction of analog VLSI information processing systems. In the *Nonlinear Circuits Handbook* from Analog Devices, we find the following clear description of a general principle by which such functions may be realized:

When compound multiplications, involving roots and powers are performed (e.g., $x_1^\alpha \times x_2^\beta \times x_3^\gamma \times x_4^\delta \times \dots$), each input is “logged,” multiplied by a constant . . . exponent of appropriate magnitude and polarity, the terms are summed and/or differenced, then the antilog is taken to convert the result back into the “world of phenomena” [1, p. 469].

A few power-law circuits that function according to this principle have been described in the literature [2]–[4]. Vittoz [4] cites Arreguit *et al.* [3] and indicates that such circuits are based on a “generalization of the translinear principle” [4, p. 37]. Arreguit *et al.*, in turn, cite the *Nonlinear Circuits Handbook* [1] and mention that in analyzing such circuits, they can “apply the generalized translinear principle that translates the sum of voltages into a product of currents and their multiplication by a constant k into the elevation of the currents to the power k ” [3, p. 443]. It seems that Arreguit *et al.* are referring to the lines just quoted from the *Nonlinear Circuits Handbook* [1]. Despite these

claims, these power-law circuits seem to have been conceived as a collection of special forms: one for powers between zero and one, one for powers greater than one, and one for negative powers.

In this paper, we present a general framework for implementing such circuits and describe intuitively the basic principles upon which they operate. We have previously described this class of circuits within the narrow context of their implementation using subthreshold floating-gate MOS (FGMOS) transistors [5]. Here, we set these circuits in a broader context and present new experimental measurements from three such circuits built from cascoded subthreshold FGMOS transistors.

II. THE MULTIPLE-INPUT TRANSLINEAR ELEMENT

Inspired originally by Shibata and Ohmi’s neuron MOS concept [6], we recently introduced a new translinear circuit primitive, called the *multiple-input translinear element* (MITE) [7], [8]. Such an element produces an output current I that is exponential in a weighted sum of its K input voltages, V_1, \dots, V_K , given by

$$I = \lambda I_s e^{(w_1 V_1 + \dots + w_k V_k + \dots + w_K V_K)/U_T} \quad (1)$$

where

- I_s pre-exponential scaling current;
- λ dimensionless constant that scales I_s proportionally;
- V_k k th input voltage;
- w_k dimensionless positive weight that scales V_k ;
- U_T thermal voltage, kT/q .

Fig. 1(a) shows a circuit symbol for an ideal K -input MITE. This symbol is meant to resemble a K -input floating-gate bipolar transistor, which of course does not exist, but the symbol is suggestive of several practical MITE implementations that we shall describe presently. We assume that the input terminals draw a negligible amount of dc current, as if they were capacitive, and that we can control the values of the weights proportionally. In many cases, we are interested primarily in the number of identical unit inputs, each with weight w , coupling an input voltage into a MITE rather than the actual weight values involved. In such cases, we omit the w associated with each of the inputs.

Fig. 1(b)–(d) show three practical implementations of the MITE, built from K -input FGMOS transistors, that we have demonstrated experimentally. For each of these FGMOS MITEs, the weights (i.e., w_1, \dots, w_K) are equal to the input capacitive divider ratios. The amount of floating-gate charge sets an electronically adjustable, nonvolatile multiplicative scale factor on the MITE’s output current (i.e., λ) that we can use to build adaptive systems or to compensate for device mismatch.

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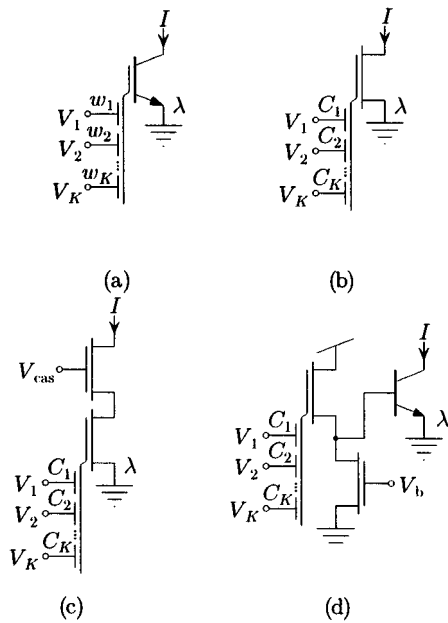


Fig. 1. Multiple-input translinear elements (MITEs). (a) Circuit symbol for an ideal K -input MITE. Such an element produces an output current that is exponential in a weighted sum of its input voltages. Parts (b)–(d) show three different MITE implementations comprising (b) a single subthreshold FG-MOS transistor, (c) a cascoded subthreshold FG-MOS transistor, and (d) a floating-gate source follower and a bipolar transistor.

We can adjust the floating-gate charge using well-characterized physical mechanisms, such as Fowler–Nordheim tunneling [9], hot-electron injection [10], and short-wave ultraviolet photoinjection [11]—such mechanisms are used routinely to program EEPROMs and flash memories.

III. BASIC MITE CIRCUIT STAGES

Consider the three basic MITE circuit stages that are depicted in Fig. 2. These three circuit stages are the building blocks from which we construct all MITE networks. The first of these circuits is a *voltage-in, current-out* (VICO) stage, shown in Fig. 2(a). Here, we apply input voltages V_i and V_k to two different input terminals of MITE Q_n , which, in response, generates an output current I_n . To see how I_n depends on V_i and V_k , using (1), we write

$$I_n \propto e^{(w_{ni}V_i + w_{nk}V_k + \dots)/U_T}.$$

By breaking out the first two terms of the weighted summation and using the fact that $e^{x+y} = e^x e^y$, we can rewrite the preceding expression as

$$I_n \propto e^{w_{ni}V_i/U_T} e^{w_{nk}V_k/U_T}. \quad (2)$$

The second of the three basic MITE stages, shown in Fig. 2(b), is a *current-in, voltage-out* (CIVO) stage. Here, we source an input current I_i into the output of MITE Q_i , and we feed the output voltage V_i back through the self-coupling weight w_{ii} . This feedback configuration adjusts V_i , so that the current sunk by MITE Q_i just balances the input current I_i . A MITE in this feedback configuration is analogous to a diode-connected transistor, so we say that it is *diode connected through* w_{ii} . To determine how the output voltage V_i depends

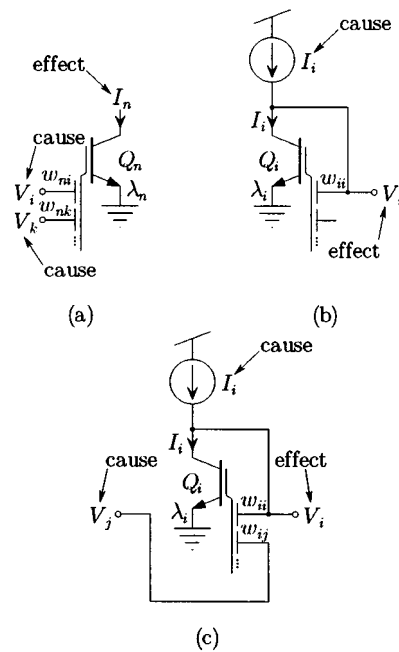


Fig. 2. Three basic circuit stages, each comprising a single MITE. (a) A voltage-in, current-out stage. (b) A current-in, voltage-out stage. (c) A voltage-in, voltage-out stage.

on the input current I_i , we begin with (1) and solve for V_i in terms of I_i . So, we write

$$I_i \propto e^{(w_{ii}V_i + \dots)/U_T}$$

which we rearrange to find that

$$V_i = \frac{U_T}{w_{ii}} \log I_i - \dots. \quad (3)$$

The third basic MITE stage is a *voltage-in, voltage-out* (VIVO) stage, shown in Fig. 2(c). This configuration is identical to the CIVO stage of Fig. 2(b), except that we now hold the current I_i fixed. We are instead concerned with how the output voltage V_i depends on an input voltage V_j , which we apply to another of the input terminals of MITE Q_i . Beginning with (1), we write that

$$I_i \propto e^{(w_{ii}V_i + w_{ij}V_j + \dots)/U_T}$$

which we rearrange to solve for V_i in terms of V_j as follows:

$$V_i = -\frac{w_{ij}}{w_{ii}} V_j - \dots. \quad (4)$$

We can use the circuit stage of Fig. 2(c) *both* as a CIVO stage *and* as a VIVO stage simultaneously. In this case, it is easy to see that V_i depends on V_j and I_i through a linear combination of (3) and (4) as follows:

$$V_i = \frac{U_T}{w_{ii}} \log I_i - \frac{w_{ij}}{w_{ii}} V_j - \dots. \quad (5)$$

IV. ELEMENTARY MITE NETWORKS

In this section, we describe two simple current-mode MITE circuits, each comprising two CIVO stages and a single VICO

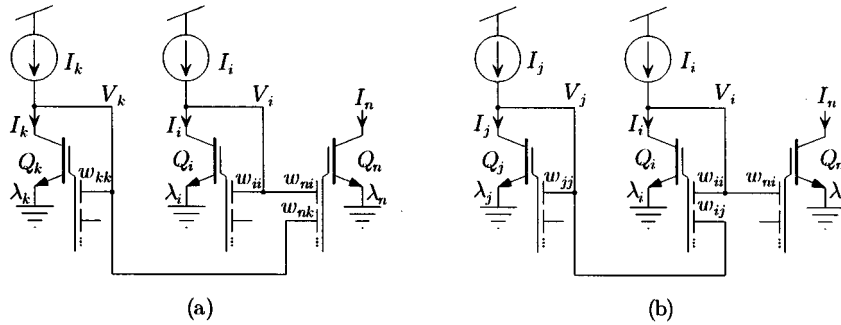


Fig. 3. Two basic current-mode circuits comprising two CIVO stages and one VICO stage. These two circuits illustrate all of the intuition underlying the class of MITE networks (a) A product-of-power-law circuit. (b) A quotient-of-power-law circuit.

stage. These two basic current-mode circuits illustrate all of the basic intuition underlying the operation of MITE networks.

In the first current-mode circuit, shown in Fig. 3(a), we connect the outputs of two different CIVO stages directly to a single VICO stage through separate inputs. To analyze this circuit, we apply (2) to the output stage, obtaining

$$I_n \propto e^{w_{ni}V_i/U_T} e^{w_{nk}V_k/U_T}. \quad (6)$$

Substituting (3) into (6) for each of V_i and V_k , we obtain

$$I_n \propto e^{w_{ni}((U_T/w_{ii}) \log I_i \dots)/U_T} e^{w_{nk}((U_T/w_{kk}) \log I_k \dots)/U_T}.$$

When we break out the first term in each of the two summations and regroup, this expression becomes

$$I_n \propto e^{(w_{ni}/w_{ii}) \log I_i} e^{(w_{nk}/w_{kk}) \log I_k}. \quad (7)$$

Note that if MITEs Q_i , Q_k , and Q_n are operating at the same temperature, then the primary temperature dependence of the relationship among I_i , I_k , and I_n disappears from (7). In this intuitive analysis, we have not kept track of the scaling currents I_s , which can be strongly temperature dependent. But, as we shall show in Section V, if the products of the input currents raised to their respective powers have units of amperes (i.e., as opposed to amperes raised to some other power than unity), then the relationship between the output current and the input currents is generally insensitive to isothermal variations. Now, because $x \log y = \log y^x$ and $e^{\log x} = x$, we can rewrite (7) as

$$I_n \propto I_i^{w_{ni}/w_{ii}} \times I_k^{w_{nk}/w_{kk}}. \quad (8)$$

Thus, the output current is proportional to the product of the two input currents, each of which is raised to a power that is set by a ratio of MITE weights.

For the second basic current-mode MITE circuit, instead of connecting the output of the second CIVO stage directly to a second input of the output VICO stage, as we did in the circuit of Fig. 3(a), we connect the output of the second CIVO stage to the output stage through the first CIVO stage, as shown in Fig. 3(b). This first CIVO stage both generates a voltage that is logarithmic in the input current I_i and serves as a VICO stage for the second CIVO stage. This connection allows us to obtain negative powers. To show that it will, we apply (1) to the output stage, obtaining

$$I_n \propto e^{(w_{ni}V_i + \dots)/U_T}. \quad (9)$$

Substituting (5) into (9), we get

$$I_n \propto e^{w_{ni}((U_T/w_{ii}) \log I_i - (w_{ij}/w_{ii})V_j \dots)/U_T}$$

into which we substitute (3) for V_j , and thus obtain

$$I_n \propto e^{w_{ni}((U_T/w_{ii}) \log I_i - (w_{ij}/w_{ii})((U_T/w_{jj}) \log I_j \dots))/U_T}.$$

Now, if we break out the first two terms of the summation and regroup, we find that

$$I_n \propto e^{(w_{ni}/w_{ii}) \log I_i} e^{-(w_{ni}/w_{ii})(w_{ij}/w_{jj}) \log I_j}. \quad (10)$$

Again, because $x \log y = \log y^x$ and $e^{\log x} = x$, we can rewrite (10) as

$$I_n \propto I_i^{w_{ni}/w_{ii}} \times I_j^{-(w_{ni}/w_{ii})(w_{ij}/w_{jj})}$$

which in turn becomes

$$I_n \propto I_i^{w_{ni}/w_{ii}} / I_j^{(w_{ni}/w_{ii})(w_{ij}/w_{jj})}. \quad (11)$$

Thus, the output current is proportional to the quotient of the two input currents, each of which is raised to a power that is set by ratios of MITE weights. Here, the powers are not completely independent of each other. However, for any value of w_{ni}/w_{ii} , we can adjust the value of w_{ij}/w_{jj} to set the power of I_j to whatever we want. This quotient-of-power-law relationship is also insensitive to isothermal variations.

These two basic current-mode MITE circuits capture all of the intuition underlying MITE network operation. We generate voltages that are logarithmic in the input currents using diode-connected MITEs. We set power laws through ratios of MITE weights and obtain negative powers by using voltage-inversion stages. We get products by summing two or more logarithmic voltages on an output MITE, which exponentiates the sum. We have formalized this intuitive analysis and have obtained systematic analysis and synthesis procedures for this class of nonlinear circuits [7].

V. MATRIX ANALYSIS OF MITE NETWORKS

Consider the general MITE network circuit, shown in Fig. 4. There are N input MITEs, labeled Q_1 through Q_N , and M output MITEs, labeled Q_{N+1} through Q_{N+M} . The collector voltage of MITE Q_k couples into the gate of MITE Q_n through the weight w_{nk} . Here, k can range from one to N and n can range from one to $N + M$. If the collector voltage of MITE

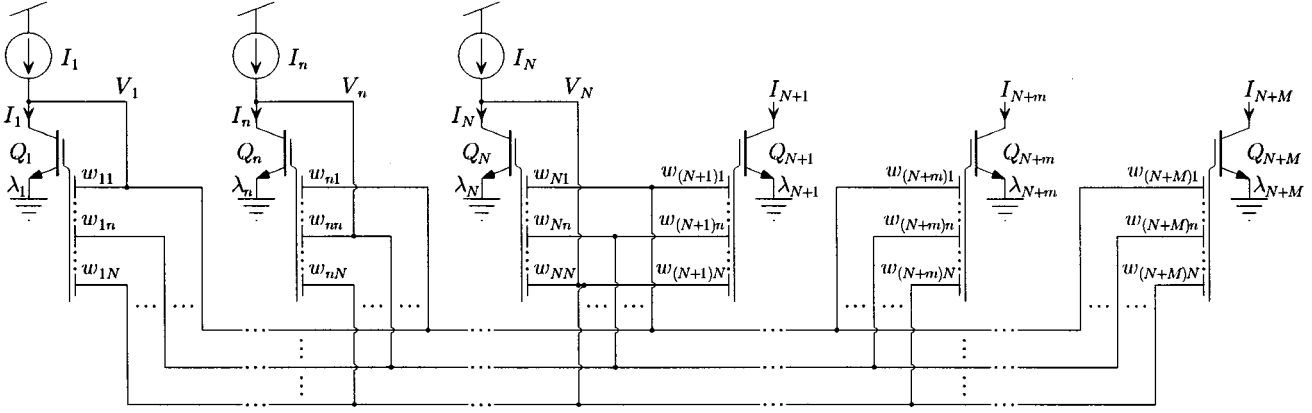


Fig. 4. Schematic of a general MITE network comprising N input MITEs, labeled Q_1 through Q_N , and M output MITEs, labeled Q_{N+1} through Q_{N+M} . Input currents I_1 through I_N are sourced into the collectors of MITEs Q_1 through Q_N , respectively, causing voltages V_1 through V_N to develop that will depend on the $N \times N$ input connectivity matrix \mathbf{W}_{in} . \mathbf{W}_{in} comprises MITE input weights w_{nk} , where both n and k can take on integer values from one to N ; the value of w_{nk} is a measure of the coupling strength between the collector voltage of MITE Q_k and the gate voltage of MITE Q_n . The circuit forms M output currents I_{N+1} through I_{N+M} by linearly combining V_1 through V_N according to the output connectivity matrix \mathbf{W}_{out} , and exponentiating. \mathbf{W}_{out} comprises MITE input weights $w_{(N+m)k}$, where m can take on integer values from one to M and k can take on integer values from one to N . The value of $w_{(N+m)k}$ is a measure of the coupling strength between the collector voltage of input MITE Q_k and the gate voltage of output MITE Q_{N+m} .

Q_k does not couple into the gate of MITE Q_n , then the value of w_{nk} is zero. Together, these weights constitute an $(N+M) \times N$ connectivity matrix \mathbf{W} . We partition \mathbf{W} into an *input connectivity matrix* \mathbf{W}_{in} and an *output connectivity matrix* \mathbf{W}_{out} . \mathbf{W}_{in} comprises the first N rows of \mathbf{W} , and \mathbf{W}_{out} comprises the last M rows of \mathbf{W} .

We source N input currents I_1 through I_N into the collectors of MITEs Q_1 through Q_N , respectively. As a result, N voltages V_1 through V_N develop that are each a linear combination of logarithms of the N input currents. The particular coefficients appearing in these linear combinations depend on the input connectivity matrix \mathbf{W}_{in} . The circuit then forms M output currents I_{N+1} through I_{N+M} in output MITEs Q_{N+1} through Q_{N+M} , respectively, by linearly combining the voltages V_1 through V_N according to the output connectivity matrix \mathbf{W}_{out} and exponentiating the resulting weighted sums. In this section, we shall show that the k th output current I_{N+m} is related to the N input currents according to

$$\frac{I_{N+m}}{\lambda_{N+m}} = I_s^{1 - \sum_{n=1}^N \Lambda_{mn}} \prod_{n=1}^N \left(\frac{I_n}{\lambda_n} \right)^{\Lambda_{mn}} \quad (12)$$

where the values of Λ_{mn} are given by the matrix product

$$\mathbf{\Lambda} \equiv \mathbf{W}_{\text{out}} \mathbf{W}_{\text{in}}^{-1}. \quad (13)$$

In other words, the k th output current is a product of the N input currents; I_n factors into the product raised to the power Λ_{nm} , which, in general, will be equal to a sum of products of ratios of MITE weight values. Now, it is easy to see that if the powers contained in $\mathbf{\Lambda}$ are such that, for each m , $\sum_{n=1}^N \Lambda_{mn} = 1$, then (12) reduces to

$$\frac{I_{N+m}}{\lambda_{N+m}} = \prod_{n=1}^N \left(\frac{I_n}{\lambda_n} \right)^{\Lambda_{mn}}$$

which is both independent of process parameters and insensitive to isothermal variations.

We shall also show that if the value of λ_n for each MITE is the same (i.e., $\lambda_1 = \dots = \lambda_{N+M} = \lambda$), then (12) further reduces to

$$I_{N+m} = \prod_{n=1}^N I_n^{\Lambda_{mn}}.$$

Finally, we shall show that if the circuit of Fig. 4 is made from MITEs that each have an identical set of weights, and if all the MITE inputs are connected to one of the V_n , then the powers in $\mathbf{\Lambda}$ are such that for each m , $\sum_{n=1}^N \Lambda_{mn} = 1$, so the I_s dependence of (12) disappears.

In the analysis that follows, we assume that all MITEs are operating at the same temperature and that they all have well-matched values of I_s . We also assume that the input connectivity matrix \mathbf{W}_{in} has an inverse $\mathbf{W}_{\text{in}}^{-1}$, so that $\mathbf{\Lambda}$ is well defined. We begin by noting that we assumed that the input terminals of the MITE draw negligible dc current, so that Kirchhoff's current law implies that, at equilibrium, the n th input current just balances the current sunk by MITE Q_n . Thus, we can apply (1) to each input MITE, and we write that

$$I_n = \lambda_n I_s e^{(w_{n1}V_1 + \dots + w_{nK}V_K)/U_T}.$$

After rearranging, taking logarithms, and solving for V_k , we obtain

$$V_k = U_T \sum_{n=1}^N (\mathbf{W}_{\text{in}}^{-1})_{kn} \log \frac{I_n}{\lambda_n I_s} \quad (14)$$

where the notation $(\mathbf{A})_{ij}$ denotes the ij th element of matrix \mathbf{A} .

From (1), the k th output current I_{N+m} is given by

$$I_{N+m} = \lambda_{N+m} I_s e^{(w_{(N+m)1}V_1 + \dots + w_{(N+m)K}V_K)/U_T}. \quad (15)$$

Substituting (14) into (15) and rearranging, we obtain

$$\begin{aligned} \frac{I_{N+m}}{\lambda_{N+m}} &= I_s \exp \left[\sum_{n=1}^N \sum_{k=1}^N w_{(N+m)k} (\mathbf{W}_{\text{in}}^{-1})_{kn} \log \frac{I_n}{\lambda_n I_s} \right] \\ &= I_s \exp \left[\sum_{n=1}^N \sum_{k=1}^N (\mathbf{W}_{\text{out}})_{mk} (\mathbf{W}_{\text{in}}^{-1})_{kn} \log \frac{I_n}{\lambda_n I_s} \right]. \end{aligned} \quad (16)$$

If we apply the definition of $\mathbf{\Lambda}$ from (13), then (16) becomes

$$\begin{aligned} \frac{I_{N+m}}{\lambda_{N+m}} &= I_s \exp \left[\sum_{n=1}^N \Lambda_{mn} \log \frac{I_n}{\lambda_n I_s} \right] \\ &= I_s \prod_{n=1}^N \exp \left[\log \left(\frac{I_n}{\lambda_n I_s} \right)^{\Lambda_{mn}} \right] \\ &= I_s \prod_{n=1}^N \left(\frac{I_n}{\lambda_n I_s} \right)^{\Lambda_{mn}} \\ &= I_s^{1-\sum_{n=1}^N \Lambda_{mn}} \prod_{n=1}^N \left(\frac{I_n}{\lambda_n} \right)^{\Lambda_{mn}}. \end{aligned} \quad (17)$$

Now, it is easy to see that if the powers contained in $\mathbf{\Lambda}$ are such that, for each m , $\sum_{k=1}^N \Lambda_{mn} = 1$, then (17) reduces to

$$\frac{I_{N+m}}{\lambda_{N+m}} = \prod_{n=1}^N \left(\frac{I_n}{\lambda_n} \right)^{\Lambda_{mn}} \quad (18)$$

which is both independent of process parameters and insensitive to isothermal variations. Moreover, if the value of λ is the same for each MITE (i.e., $\lambda_1 = \dots = \lambda_{N+M} = \lambda$), then we have that

$$I_{N+m} = \lambda^{1-\sum_{n=1}^N \Lambda_{mn}} \prod_{n=1}^N I_n^{\Lambda_{mn}} = \prod_{n=1}^N I_n^{\Lambda_{mn}}.$$

These results were just what we set out to show.

Now, if each of the $N + M$ MITEs in the circuit of Fig. 4 has an identical set of K weights w_1 through w_K such that $\sum_{k=1}^K w_k = w_T$, where w_T is a constant. If each MITE input is connected to one of the N input node voltages V_1 through V_N , then it is easy to see that these conditions imply that the sum of each of the rows of the connectivity matrix \mathbf{W} sums to the constant w_T (i.e., for each n between one and $N + M$, $\sum_{k=1}^N w_{nk} = w_T$). In the Appendix, we show that this condition on \mathbf{W} is sufficient to guarantee that $\mathbf{\Lambda}$ is such that, for each m between one and M , $\sum_{n=1}^N \Lambda_{mn} = 1$, which in turn implies that (17) reduces to (18). Note that this condition on \mathbf{W} is *not* a necessary one; each of the rows of $\mathbf{\Lambda}$ may sum to unity even though the rows of \mathbf{W} do not sum to the same quantity.

VI. EXPERIMENTAL RESULTS

In this section, we show experimental measurements from three MITE networks—a geometric-mean circuit, a

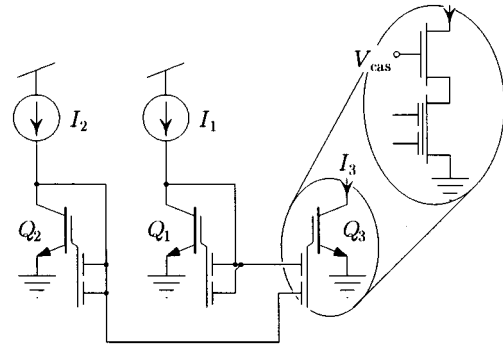


Fig. 5. A two-input geometric-mean circuit comprising three two-input MITEs. Each MITE was implemented as a cascoded subthreshold FG MOS transistor, as shown in Fig. 1(c). The cascode voltage was fixed at 0.8 V, and the floating-gate charges were balanced by ultraviolet (UV) photoinjection.

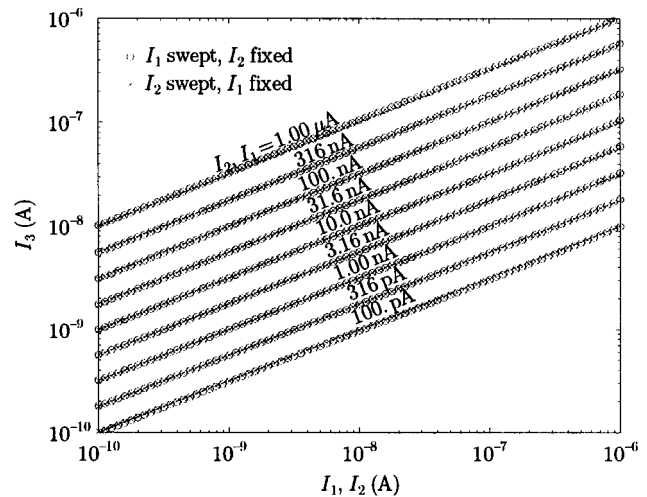


Fig. 6. Measured data from the circuit of Fig. 5. Circles are measured values of I_3 plotted as a function of I_1 for various values of I_2 . Points marked by \times show measured values of I_3 plotted as a function of I_2 for various values of I_1 . Solid lines show the ideal expression, $I_3 = \sqrt{I_1 I_2}$, calculated from the values of I_1 and I_2 at each point.

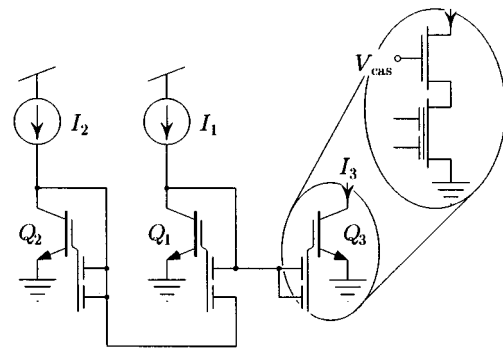


Fig. 7. A squaring-reciprocal circuit comprising three two-input MITEs. Each MITE was implemented as a cascoded subthreshold n-channel FG MOS transistor, as shown in Fig. 1(c). The cascode voltage was fixed at 0.8 V, and the floating-gate charges were balanced by UV photoinjection.

squaring-reciprocal circuit, and a one-quadrant multiply-reciprocal circuit—that were fabricated in a 1.2- μm double-poly n-well CMOS process. For each of these circuits, we implemented the MITEs as cascoded subthreshold n-channel FG MOS transistors, as shown in Fig. 1(c), with two identical control gates of about 210 fF each. Both the cascode transistor

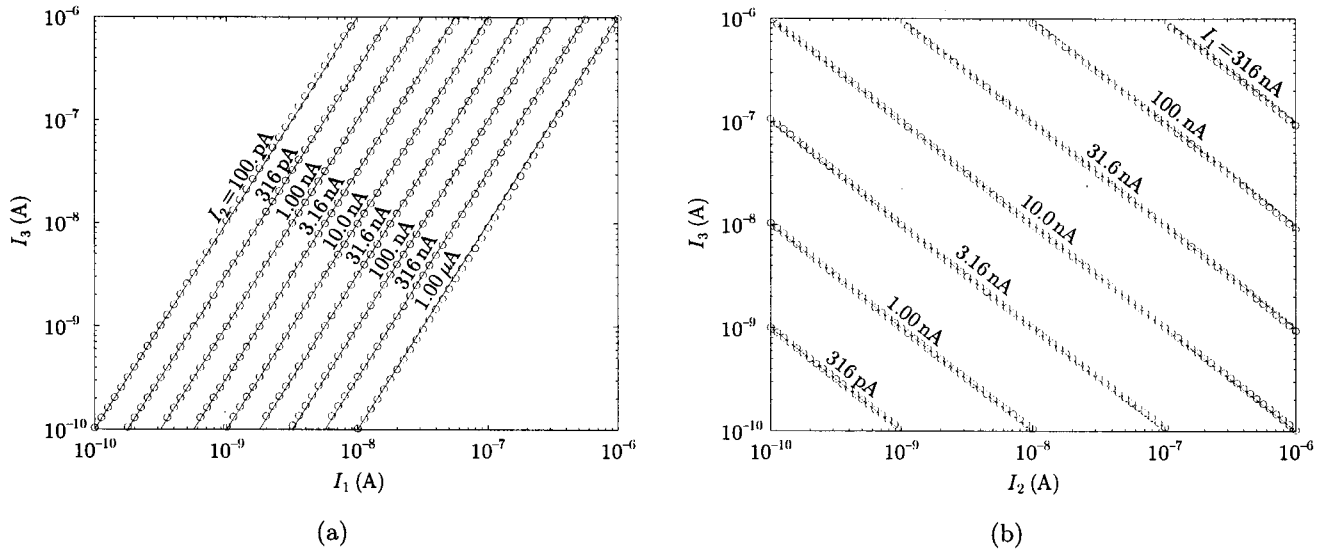


Fig. 8. Measured data from the circuit of Fig. 7. Circles are measured values of I_3 plotted as a function of (a) I_1 for various values of I_2 and (b) I_2 for various values of I_1 . Solid lines show the ideal expression, $I_3 = I_1^2 / I_2$, calculated from the values of I_1 and I_2 at each point.

and the FG MOS transistor were $216 \mu\text{m}$ wide and $3.6 \mu\text{m}$ long. We used such wide transistors both to ensure good matching and to extend the subthreshold current range up to approximately $1 \mu\text{A}$ to facilitate measurement. These circuits function in the same way with much smaller transistors, although device mismatch would be more pronounced and the current range over which they function would be somewhat smaller. We balanced the floating-gate charges by shorting all of the pins on the chip together and exposing the chip to short-wave ultraviolet light. Consequently, we expect that each MITE will have the same value of λ . We fixed the cascode bias voltage at 0.8 V for all measurements.

A. Geometric-Mean Circuit

Consider the circuit shown in Fig. 5, consisting of three two-input MITEs. Taking the weight of each control gate to be w , we have that

$$\mathbf{W}_{\text{in}} = \begin{bmatrix} 2w & 0 \\ 0 & 2w \end{bmatrix} \quad \text{and} \quad \mathbf{W}_{\text{out}} = [w \quad w]$$

from which we find that

$$\mathbf{W}_{\text{in}}^{-1} = \begin{bmatrix} \frac{1}{2w} & 0 \\ 0 & \frac{1}{2w} \end{bmatrix}$$

and

$$\mathbf{\Lambda} = \mathbf{W}_{\text{out}} \mathbf{W}_{\text{in}}^{-1} = [w \quad w] \begin{bmatrix} \frac{1}{2w} & 0 \\ 0 & \frac{1}{2w} \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & \frac{1}{2} \end{bmatrix}.$$

Thus, the circuit of Fig. 5 embodies the two-input geometric-mean relationship

$$I_3 = \sqrt{I_1 I_2}. \quad (19)$$

Fig. 6 shows measured data from the circuit of Fig. 5. Circles represent measured values of I_3 plotted as a function of I_1 over

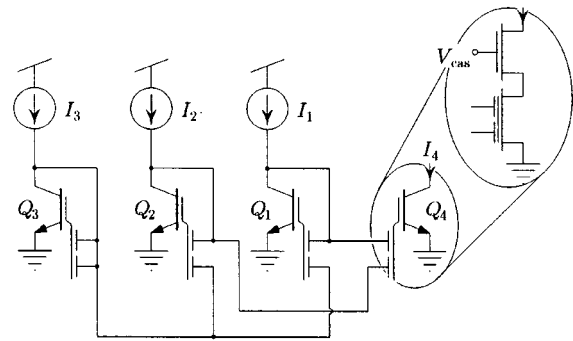


Fig. 9. A one-quadrant multiply-reciprocal circuit comprising four two-input MITEs. Each MITE was implemented as a cascoded subthreshold FG MOS transistor, as shown in Fig. 1(c). The cascode voltage was fixed at 0.8 V , and the floating-gate charges were balanced by UV photoinjection.

the four-decade current range from 100 pA to $1 \mu\text{A}$ for nine different values of I_2 ranging from 100 pA to $1 \mu\text{A}$. Points marked by \times point markers correspond to measured values of I_3 plotted as a function of I_2 for nine different values of I_1 over the same range of currents. Straight lines show values of I_3 calculated from (19) using the values of I_1 and I_2 at each point. The data and fits agree well over the entire range of input currents.

B. Squaring-Reciprocal Circuit

Consider the circuit shown in Fig. 7, consisting of three two-input MITEs. Taking the weight of each control gate to be w , we have that

$$\mathbf{W}_{\text{in}} = \begin{bmatrix} w & w \\ 0 & 2w \end{bmatrix} \quad \text{and} \quad \mathbf{W}_{\text{out}} = [2w \quad 0]$$

from which we find that

$$\mathbf{W}_{\text{in}}^{-1} = \begin{bmatrix} \frac{1}{w} & -\frac{1}{2w} \\ 0 & \frac{1}{2w} \end{bmatrix}$$

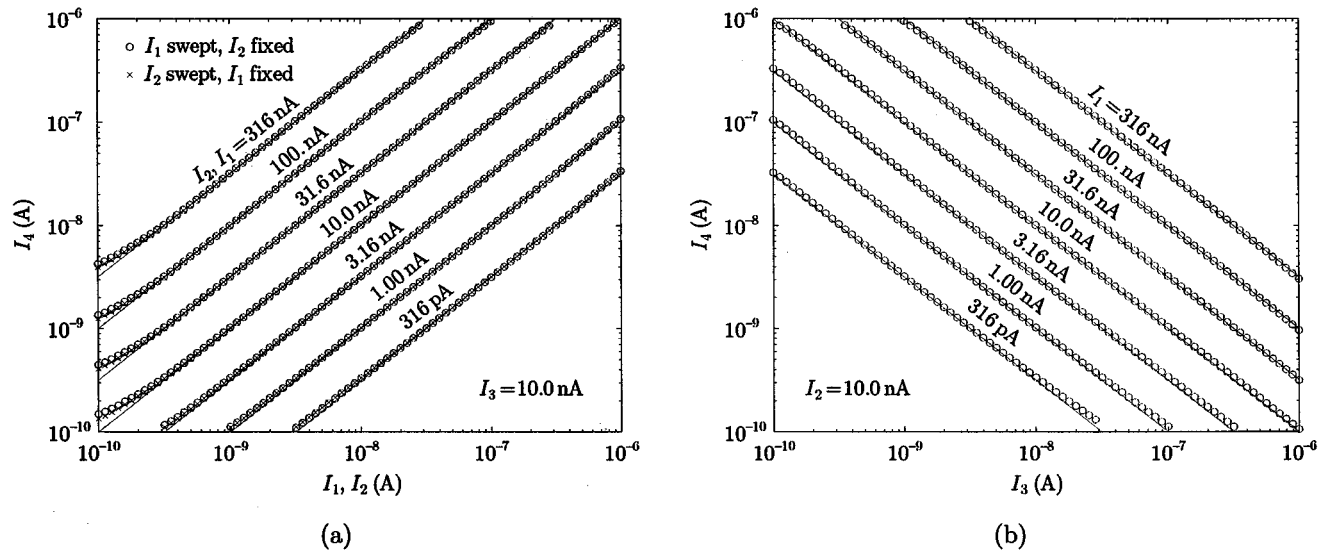


Fig. 10. Measured data from the circuit of Fig. 9. (a) Circles are measured values of I_4 plotted as a function of I_1 for various values of I_2 and I_3 fixed at 10 nA. Points marked by \times show measured values of I_4 plotted as a function of I_2 for various values of I_1 with I_3 fixed at 10 nA. (b) Circles show measured values of I_4 plotted as a function of I_3 for various values of I_1 with I_2 fixed at 10 nA. In each case, solid lines show the ideal expression, $I_4 = I_1 I_2 / I_3$, calculated from the values of I_1 , I_2 , and I_3 at each point.

and

$$\Lambda = \mathbf{W}_{\text{out}} \mathbf{W}_{\text{in}}^{-1} = [2w \quad 0] \begin{bmatrix} \frac{1}{w} & -\frac{1}{2w} \\ 0 & \frac{1}{2w} \end{bmatrix} = [2 \quad -1].$$

Thus, the circuit of Fig. 7 implements the squaring/reciprocal relationship

$$I_3 = \frac{I_1^2}{I_2}. \quad (20)$$

Fig. 8 shows measured data from the circuit of Fig. 7. The circles shown in Fig. 8(a) represent measured values of I_3 plotted as a function of I_1 over the four-decade current range from 100 pA to 1 μ A for nine different values of I_2 ranging from 100 pA to 1 μ A. The circles shown in Fig. 8(b) correspond to measured values of I_3 plotted as a function of I_2 for nine different values of I_1 over the same range of currents. In both cases, the straight lines show values of I_3 calculated from (20) using the values of I_1 and I_2 at each point. The data and fits agree well over the entire range of input currents. Fig. 10 shows measured data from the circuit of Fig. 9. The circles shown in Fig. 10(a) represent measured values of I_4 plotted as a function of I_1 over the four-decade current range from 100 pA to 1 μ A for seven different values of I_2 and I_3 fixed at 10 nA. The points marked by \times point markers in Fig. 10(a) correspond to measured values of I_4 plotted as a function of I_2 for seven different values of I_1 and I_3 fixed at 10 nA. The circles shown in Fig. 10(b) correspond to measured values of I_4 plotted as a function of I_3 for seven different values of I_1 with I_2 fixed at 10 nA. In each case, straight lines show values of I_4 calculated from (21) using the values of I_1 , I_2 , and I_3 at each point. The data and fits agree well over much of the range shown; deviations at low current levels in Fig. 10(a) arise because the cascode transistor in MITE Q_1 (circles) or MITE Q_2 (\times point markers) was not saturated.

C. Multiply-Reciprocal Circuit

Consider the circuit shown in Fig. 9, which we have published previously [7], consisting of four two-input MITEs. Taking the weight of each control gate to be w , we have that

$$\mathbf{W}_{\text{in}} = \begin{bmatrix} w & 0 & w \\ 0 & w & w \\ 0 & 0 & 2w \end{bmatrix} \quad \text{and} \quad \mathbf{W}_{\text{out}} = [w \quad w \quad 0]$$

from which we find that

$$\mathbf{W}_{\text{in}}^{-1} = \begin{bmatrix} \frac{1}{w} & 0 & -\frac{1}{2w} \\ 0 & \frac{1}{w} & -\frac{1}{2w} \\ 0 & 0 & \frac{1}{2w} \end{bmatrix}$$

and

$$\begin{aligned} \Lambda &= \mathbf{W}_{\text{out}} \mathbf{W}_{\text{in}}^{-1} \\ &= [w \quad w \quad 0] \begin{bmatrix} \frac{1}{w} & 0 & -\frac{1}{2w} \\ 0 & \frac{1}{w} & -\frac{1}{2w} \\ 0 & 0 & \frac{1}{2w} \end{bmatrix} \\ &= [1 \quad 1 \quad -1]. \end{aligned}$$

Thus, the circuit of Fig. 9 embodies the one-quadrant product/reciprocal relationship

$$I_4 = \frac{I_1 I_2}{I_3}. \quad (21)$$

VII. CONCLUSIONS

We have described a class of translinear circuits, called MITE networks, that accurately implement product-of-power-law relationships among a set of input currents. MITEs are simply implemented using multiple-input FGMOS transistors. For such MITE implementations, the power laws are determined by ratios of control-gate capacitances, and so can be made quite accurate by careful layout. Additionally, for MITE networks implemented with FGMOS transistors, the quantity of charge stored on the floating gates sets an electronically adjustable, nonvolatile multiplicative scale factor on each output current of a MITE network that we can use to build adaptive systems or to compensate for device mismatch.

We have presented a simple procedure for analyzing the product-of-power-law relationships embodied in any given MITE network using input and output connectivity matrices. We also presented experimental data from three different MITE networks that were fabricated in a 1.2- μm double-poly n-well CMOS process.

APPENDIX

In this Appendix, we shall show that if the rows of \mathbf{W} sum to the same constant w_T (i.e., for each n between one and $N+M$, $\sum_{k=1}^N w_{nk} = w_T$), and if the input connectivity matrix \mathbf{W}_{in} is invertible, then the powers contained in $\mathbf{\Lambda}$ will be such that for each m , $\sum_{n=1}^N \Lambda_{mn} = 1$. The following theorem will prove useful for this endeavor.

Theorem 1: If each of the rows of an invertible matrix \mathbf{A} sums to some constant C , then each of the rows of \mathbf{A}^{-1} sums to the constant $1/C$.

Proof: The condition that the sum of each of the rows of \mathbf{A} sums to some constant C can be written in matrix notation as follows:

$$\mathbf{A} \begin{bmatrix} 1 \\ \vdots \\ 1 \end{bmatrix} = C \begin{bmatrix} 1 \\ \vdots \\ 1 \end{bmatrix}.$$

Now, we premultiply each side of the preceding equation by \mathbf{A}^{-1} to obtain

$$\mathbf{A}^{-1}\mathbf{A} \begin{bmatrix} 1 \\ \vdots \\ 1 \end{bmatrix} = C\mathbf{A}^{-1} \begin{bmatrix} 1 \\ \vdots \\ 1 \end{bmatrix}$$

which implies that

$$\mathbf{I} \begin{bmatrix} 1 \\ \vdots \\ 1 \end{bmatrix} = C\mathbf{A}^{-1} \begin{bmatrix} 1 \\ \vdots \\ 1 \end{bmatrix}$$

where \mathbf{I} is the $N \times N$ identity matrix. We simply rewrite the preceding equation as

$$\mathbf{A}^{-1} \begin{bmatrix} 1 \\ \vdots \\ 1 \end{bmatrix} = \frac{1}{C} \begin{bmatrix} 1 \\ \vdots \\ 1 \end{bmatrix}$$

which is just what we set out to show, written in matrix notation. ■

Now, suppose that the rows of \mathbf{W} sum to w_T (i.e., for each n between one and $N+M$, $\sum_{k=1}^N w_{nk} = w_T$) and consider the quantity

$$\begin{aligned} \sum_{n=1}^N \Lambda_{mn} &= \sum_{n=1}^N \sum_{k=1}^N (\mathbf{W}_{\text{out}})_{mk} (\mathbf{W}_{\text{in}}^{-1})_{kn} \\ &= \sum_{k=1}^N (\mathbf{W}_{\text{out}})_{mk} \sum_{n=1}^N (\mathbf{W}_{\text{in}}^{-1})_{kn} \\ &= \sum_{k=1}^N (\mathbf{W}_{\text{out}})_{mk} \left(\frac{1}{w_T} \right) \\ &= \frac{1}{w_T} \sum_{k=1}^N (\mathbf{W}_{\text{out}})_{mk} \\ &= \frac{w_T}{w_T} \\ &= 1 \end{aligned}$$

which is what we set out to show.

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